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METEOR BURST COMMUNICATIONS IMPROVEMENT STUDY

ITT Aerospace/Communications Division

David Peterson

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13. ABSTRACT (Maximum 200 words) <p>Two identical Meteor Burst Radio Terminals were developed, fabricated and delivered to the Air Force. Each is controlled by a PC computer in a memo driven manner. Mode of operation is full duplex. The RF frequency range is 40 to 60 MHz with tuning increments of 25 KHz. Data rates are 4, 8, 16, 32, 64, 128, 256, and 512 kbps. Modulation is coherent Binary Phase Shift Keying (BPSK) and incoherent Differential Phase Shift Keying (DPSK). Protocol includes Automatic Repeat Request (ARQ) with source and destination addressing, message number, start of message and end of message. Messages are packetized and Read Solomon (R-S) coding is an option. The ARQ is under control of a Cyclic Redundancy Check Code (CRCC) which detects binary errors within each packet. The terminal is intended to increase meteor trail availability and data throughput by several orders of magnitude - by operating with new antennas that provide much higher gains without sacrificing meteor trail acquisition performance.</p>				
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SECTION 1

INTRODUCTION AND SUMMARY

This Final Report describes the work that was performed under the Meteor Burst Communications Improvement Study program to improve the throughput performance of a meteor burst communication link by developing a meteor burst modem that can operate at very high burst data rates.

1.1 Program Objectives

Studies [1] have shown that the instantaneous bandwidth of the meteor burst communications channel is very wide (greater than 1 MHz) and that the channel is capable of supporting data rates greater than 1 Mbps. Existing meteor burst communication systems operate at data rates from 2 to 128 kbps, which is well below the bandwidth limitations of the meteor burst channel. These data rates were selected to minimize the time delay between usable meteor trails when operating with a conventional meteor burst system. However, with the development of very high gain, adaptive, meteor burst antennas, much higher data rates are needed to utilize the available channel capacity when strong underdense or overdense trails occur. Since the majority of the meteor burst channel capacity occurs on these relatively infrequent, strong underdense and overdense trails, the full potential of a meteor burst communication system can't be realized unless it can operate at very high burst data rates. The modems developed on this program address this problem by providing the capability to operate at burst data rates up to 512 kbps; 4 times higher than any previously reported meteor burst system [2].

The primary objectives of the Meteor Burst Communications Improvement Study program were as follows:

1. Investigate system trade-offs, in the areas of modulation, error control coding and link protocol to maximize the throughput that can be achieved over a meteor burst link.
2. Develop and deliver a pair of experimental meteor burst modems capable of operating at data rates from 4 to 512 kbps.

3. Ultimately, test the modems in an operational link to measure the throughput performance that can be achieved in practice when operating at very high burst data rates.

1.2 Program Description

The Meteor Burst Communications Improvement Study program was carried out in two phases; a 12 month study phase followed by a brassboard development and test phase. The initial study phase started in January 1989 and was completed in December of that year. The results of the system trade-off study and a recommended design approach for the brassboard modems were documented in a Design Plan [3] that was submitted to the Government in November of 1989. A joint design review between ITT and the Government was held in January 1990. At that time, the Government approved the design but requested that instrumentation be added to the modems so that the amplitude and duration of meteor trails could automatically be measured and recorded. The Government also requested that acceptance tests be conducted with a government furnished meteor burst channel simulator. A contract modification to cover the additional work and extend the contract delivery date to March 1991 was awarded in May of 1990.

Detailed hardware and software design began in the spring of 1990. During the development phase, difficulties were encountered in meeting the real time processing requirements, when operating at the maximum burst data rate of 512 kbps. These difficulties delayed completion of the modems, but were finally resolved through optimization of the hardware and software design to increase the processing speed of the meteor burst controller. The causes of these problems and changes that were made to correct them are described in sections 4 and 5. The two brassboard modems, developed on this program, were completed and shipped to Science Applications International Corporation (SAIC) in November 1992 where they are now being integrated into a meteor burst demonstration system that will be field tested later this year.

1.3 System Description

As shown in Figure 1.3-1, the meteor burst modem consists of two major components; a control terminal and the modem assembly. The control terminal is a PC-AT compatible computer that connects to the modem assembly via a standard RS-232 serial interface. The control terminal provides a menu oriented display through which the operator can select the desired mode of operation, enter test messages, and monitor status. The

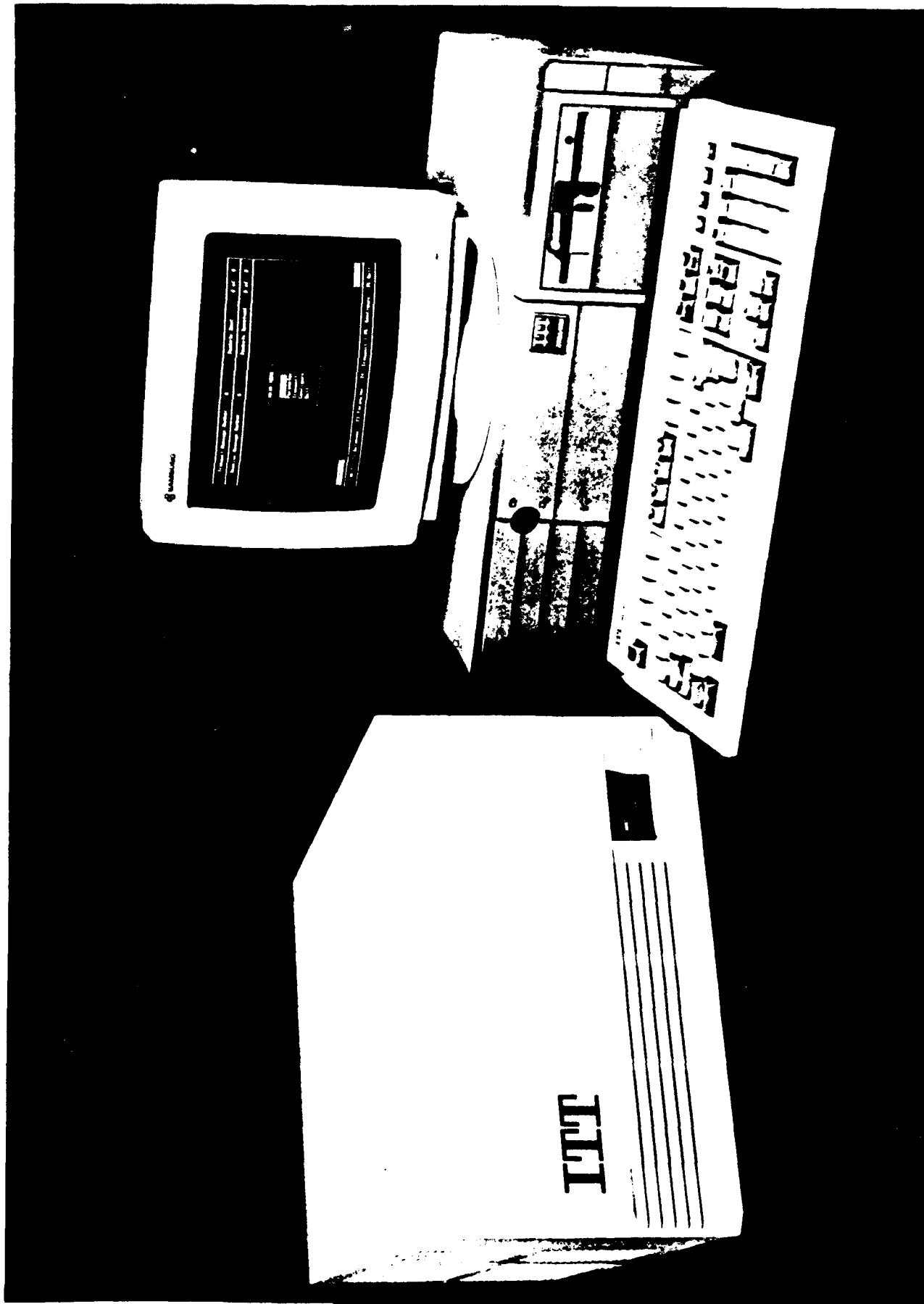


Figure 1 3-1 Photo of Meteor Burst Modem and Control Terminal

modem assembly consists of a VMEbus chassis, which house a single board computer, a multimode digital demodulator, a power supply, and a full-duplex VHF transmitter and receiver.

A top level block diagram of the modem, showing the key functional areas and the interfaces between them is given in Figure 1.3-2. Notice that the modem is divided into three sections; the modem controller and receive demodulator section, an RF section, and the power supply. The modem controller is an, off-the-shelf, single board computer (SBC) that formats and decodes all transmit and receive messages. It also interfaces with the control terminal and an optional Bit-Error-Rate (BER) test set and controls the operation of all other boards in the modem. The transmit and receive baseband/control board contains all the custom interface circuitry needed to buffer transmit data going from the SBC to the transmit modulator and receive data coming from the digital demodulator to the SBC. The baseband/control board also contains the custom interface circuitry required by the SBC to control the digital demodulator and RF sections of the modem. The multimode digital demodulator consists of 5 custom developed VMEbus expansion cards that house the receive correlator, multimode digital matched filter, and bit synchronizer portions of the modem design. It processes analog baseband information from the IF module and recovers the receive data and clock when operating at any data rate from 4 to 512 kbps.

The RF section of the modem is composed of five modules; tuner, IF module, transmit synthesizer, receive synthesizer, and transmit modulator. The tuner accepts receive RF signals within the 40 to 60 MHz frequency range and downconverts them to a 10.7 MHz IF by mixing with a local oscillator (LO) signal from the receive synthesizer module. The IF module amplifies and filters the low level signals from the tuner module and converts them to in-phase (I) and quadrature (Q) baseband signals, which are then supplied to the digital demodulator. The IF module also provides a detected RF output level that can be used to monitor trail wave shapes and noise levels on an oscilloscope or strip charter recorder. The transmit modulator accepts an unmodulated RF carrier from the transmit synthesizer and generates a biphasic modulated carrier, which is provided as an RF output from the modem.

1.4 Performance Specifications

The key performance specifications for the brassboard modem are summarized in Table 1.4-1. Notice that the transmit and receive data rates are operator selectable in octave steps from 4 to 512 kbps. Full duplex, transmit and receive, operation is provided over the

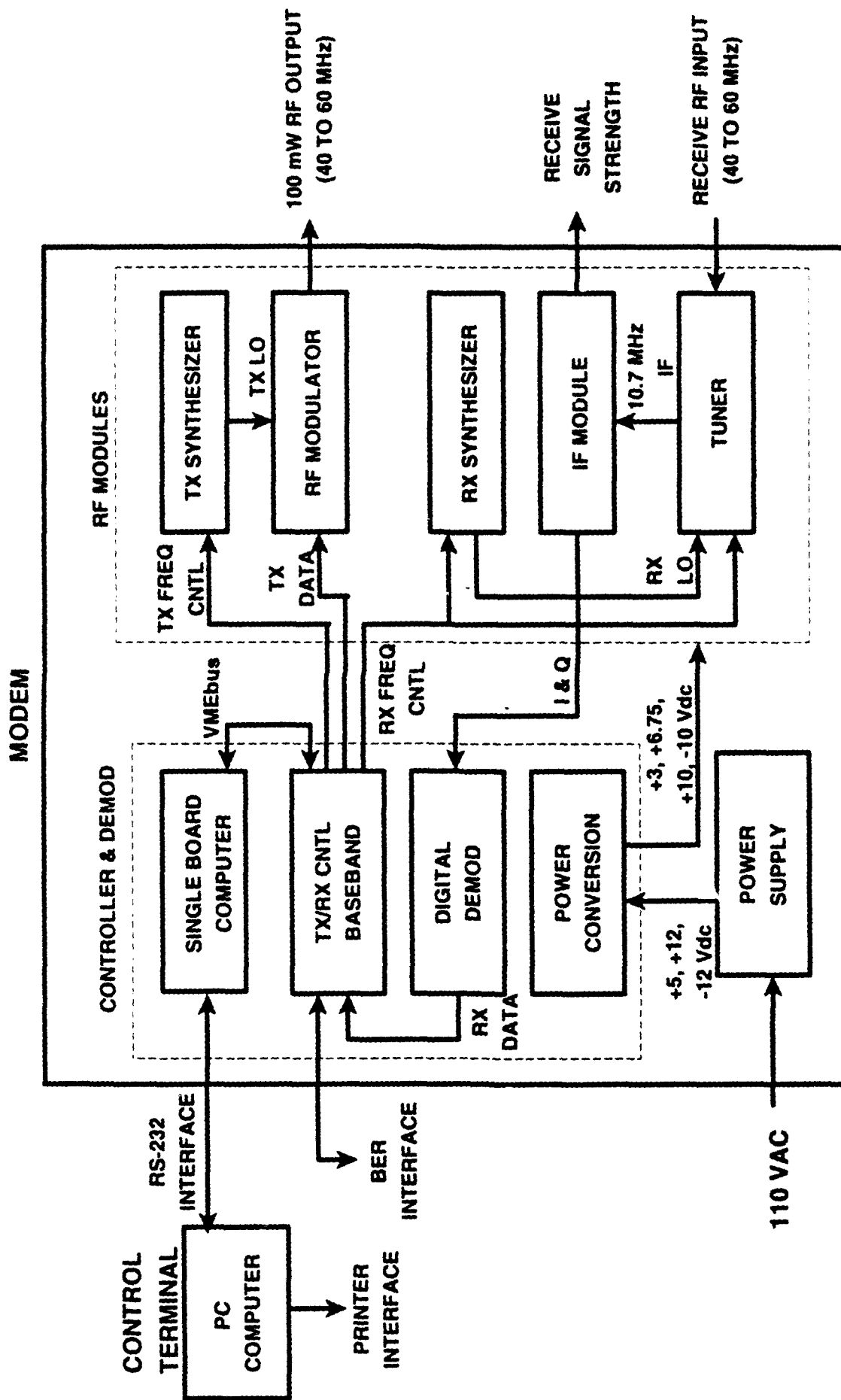


Figure 1.3-2 Modem Block Diagram

frequency range from 40 to 60 MHz. Both coherent and noncoherent modulation modes are included in the modem. An RF output power level of +20 dBm is provided for laboratory tests or to drive an external RF power amplifier.

Item	Specification
Mode of Operation	Full Duplex
RF Frequency	40 to 60 MHz (tunable in 25 kHz increments)
Frequency Accuracy	± 2 PPM
Transmit Power	+20 dBm into 50 Ohms
Receiver:	
Noise Figure	7.5 dB max
Image Rejection	80 dB min
<u>IF Filter Bandwidth:</u>	
Data Rate ≥ 256 kbps	3 dB Bandwidth = 1 MHz
Data Rate ≤ 128 kbps	3 dB Bandwidth = 256 kHz
<u>Baseband LPF Bandwidth:</u>	
Data Rate ≥ 128 kbps	3 dB Bandwidth = 1 MHz
Data Rate ≤ 64 kbps	3 dB Bandwidth = $.2 \cdot \text{Data Rate}$
<u>Sensitivity:</u> *	
Data Rate = 512 kbps	10^{-2} BER @ -103 dBm
Data Rate = 64 kbps	10^{-2} BER @ -112 dBm
Data Rate = 8 kbps	10^{-2} BER @ -121 dBm
Channel Data Rate	4, 8, 16, 32, 64, 128, 256, 512 kbps
Modulation:	
Coherent	Differentially Encoded Binary PSK (DBPSK)
Noncoherent	Differential PSK (DPSK)
Forward Error Control Coding:	
Data Packets	Reed-Solomon (31,23)
Control Frames	Shortened RS (13,9) Using 5-Bit RS Symbols
Link Protocol	Fixed Rate, Hybrid ARQ **
Control Interface	RS-232 Serial Interface @ 9.6 kbps

* When operating in BPSK mode without FEC coding.

** See section 2 for protocol definition.

Table 1.4-1 Modem Specifications

1.5 System Performance

This section presents measured test results on the acquisition time and throughput performance of the brassboard modems when operating at different burst data rates. These parameters indicate how efficiently the modems operate when transferring information over a meteor burst link.

Link Acquisition Time

Link acquisition time is defined as the time from the start of a trail until the modems are ready to begin sending the first packet of data. During this time, both modems must establish sync, identify the responding station, and determine the last consecutive data packet successfully received by the responding station on the previous trail. Once this handshaking is completed, the modems are ready to begin sending data packets.

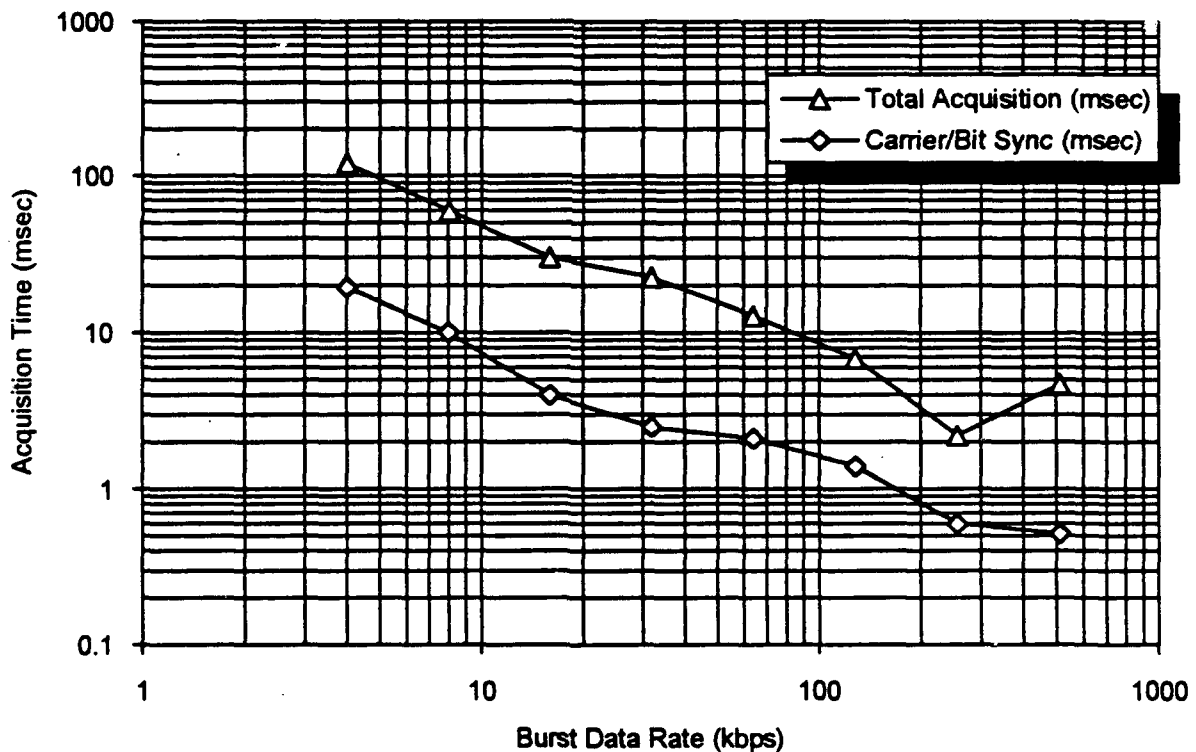


Figure 1.5-1 Link Acquisition Time

The acquisition times, measured on the brassboard modems, are plotted as a function of burst data rate in Figure 1.5-1. The results show that link acquisition time decreases as burst data rate goes from 4 to 256 kbps and then begins to increase as the data rate goes from 256 to 512 kbps. This increase in acquisition time occurs when the receive

data rate exceeds the real-time processing capability of the modem controller causing a slight delay in the response time of the modem. As will be shown later in this section, this increase in acquisition time is small enough that it has a negligible effect on the throughput performance of the modems at 512 kbps.

The acquisition times of the receive demodulator carrier tracking loop and bit sync network are also shown in Figure 1.5-1. These times are typically less than 10% of the total acquisition time and therefore have little effect on the throughput performance of the system.

Minimum Trail Duration

The minimum trail duration required to send a single packet of data is shown in Figure 1.5-2. These times were measured by adjusting the time duration of trails provided by a meteor burst channel simulator until only one packet of data was received on each trail. As expected, the trail duration required to send a single data packet decreases as a function of burst data rate. A slight increase in the minimum trail duration occurs at 512 kbps due to the increase in link acquisition time that was discussed previously.

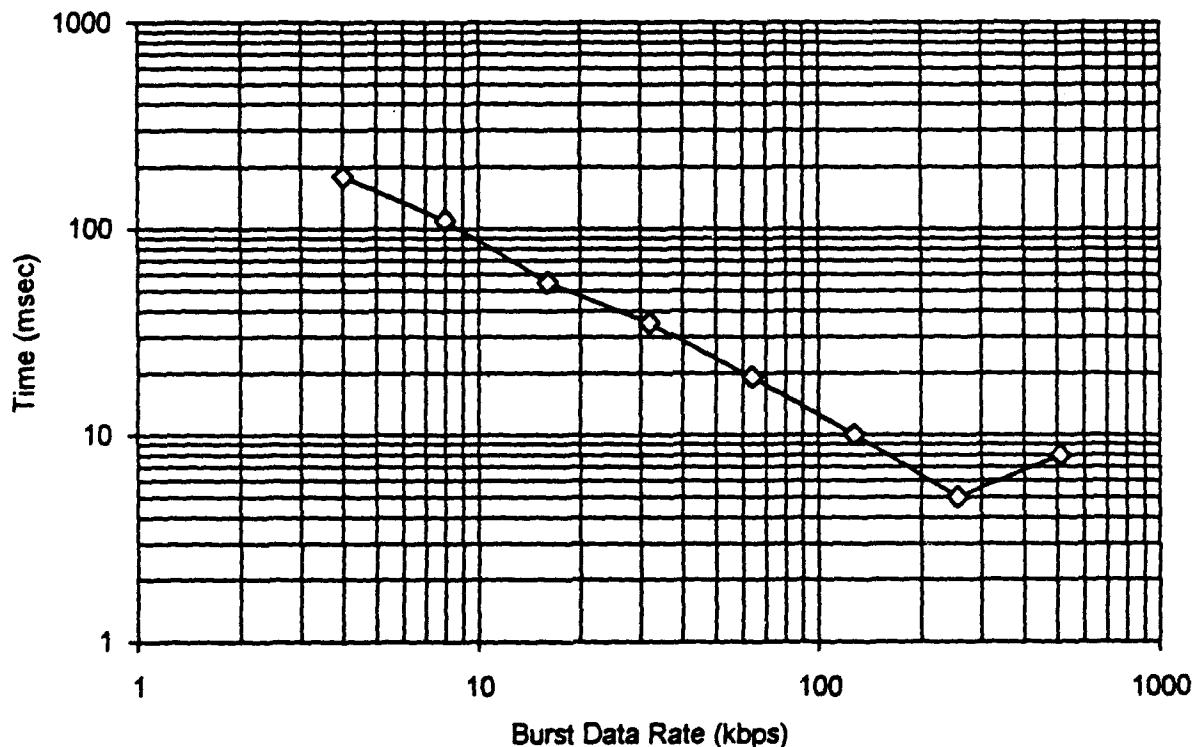


Figure 1.5-2 Minimum Trail Duration Required to Send 1 Packet of Data

Throughput Performance

Figure 1.5-3 shows the throughput performance of the modems when operating at a constant E_b/N_o of 16 dB with a trail duration of 500 ms. At this signal-to-noise ratio (SNR) with the RS CODEC enabled, there should be no uncorrected errors in the receive data so no data packets should have to be repeated. Under these conditions, throughput is determined by the percentage of the trail taken up by link acquisition and the percentage of overhead bits associated with link protocol and forward error control (FEC) coding.

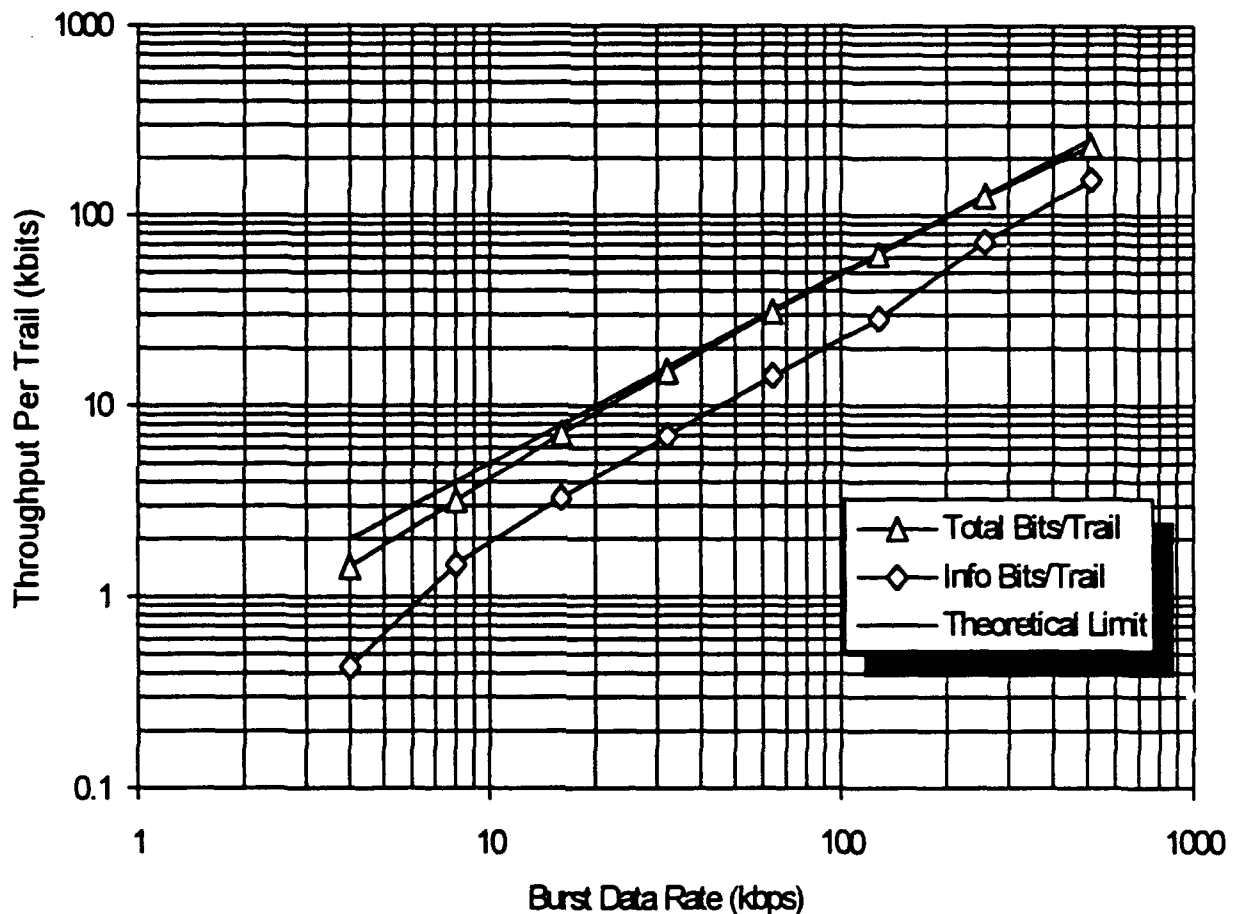


Figure 1.5-3 Throughput Per Trail When Operating @ an E_b/N_o of 16 dB With a Trail Duration of 500 ms and the Reed-Solomon CODEC Enabled

The curve labeled "Theoretical Limit" in Figure 1.5-3 shows the maximum number of bits that could be received in 500 ms if the acquisition time was zero and the system had no overhead. A second curve labeled "Total Bits/Trail" shows the total number of bits actually received in 500 ms. This includes the bits contained in the packet headers plus the bits in the data packets themselves. The third curve, labeled "Info Bits/Trail" shows the

number of information bits received in a 500 ms trail. In this case, only the information bits contained in the data packets were counted as throughput. Similar test results, measured with a trail duration of 200 ms, are given in Figure 1.5-4.

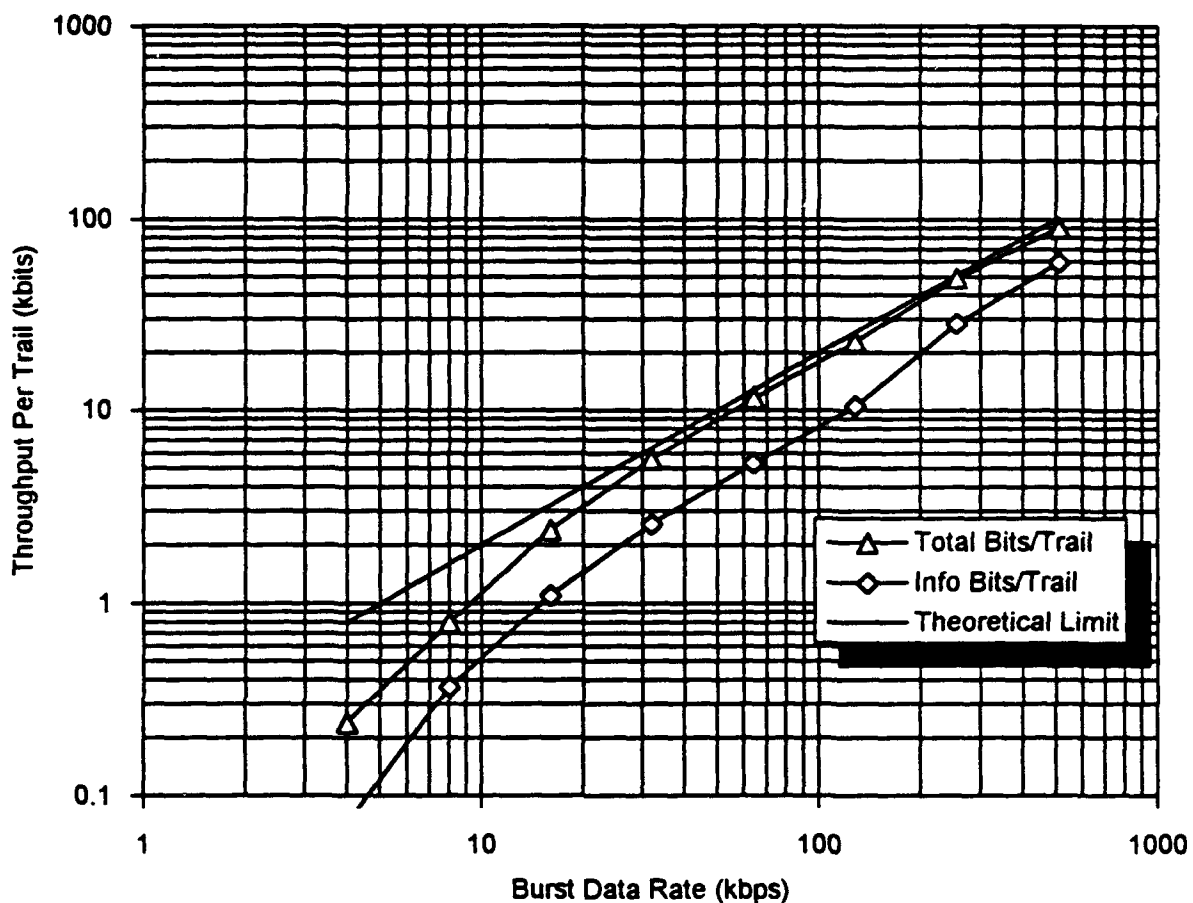


Figure 1.5-4 Throughput Per Trail When Operating @ an E_b/N_o of 16 dB With a Trail Duration of 200 ms and the Reed-Solomon CODEC Enabled

Link Efficiency

The efficiency of the modems in terms of how well they make use of the available trail duration can be calculated as follows:

$$\text{Link Efficiency} = \frac{\text{Information Bits Per Trail}}{\text{Trail Duration} \times \text{Data Rate}}$$

Link efficiency is plotted as a function of burst data rate in Figure 1.5-5. Two interesting conclusions can be drawn from this figure:

1. At the lower data rates, link efficiency is primarily determined by the percentage of the trail required for link acquisition. Under these conditions, link efficiency is directly related to the length of the trail. This is the reason that link efficiency more than doubles at 4 kbps as trail duration increases from 200 to 500 ms.
2. At the higher data rates, link efficiency is primarily determined by the percentage of overhead associated with FEC and the packet protocol. Since the modem uses a 3/4 rate RS code for data packets, the overhead due to FEC limits the maximum link efficiency to less than 75%. The difference between the 75% maximum link efficiency and measured test results is due to the overhead added by packet headers. The abrupt increase in link efficiency that occurs as the data rate goes from 128 kbps to 256 kbps is due to the increase in packet length at data rates of 256 kbps and above. (See section 2.2 for a definition of packet lengths versus data rate.)

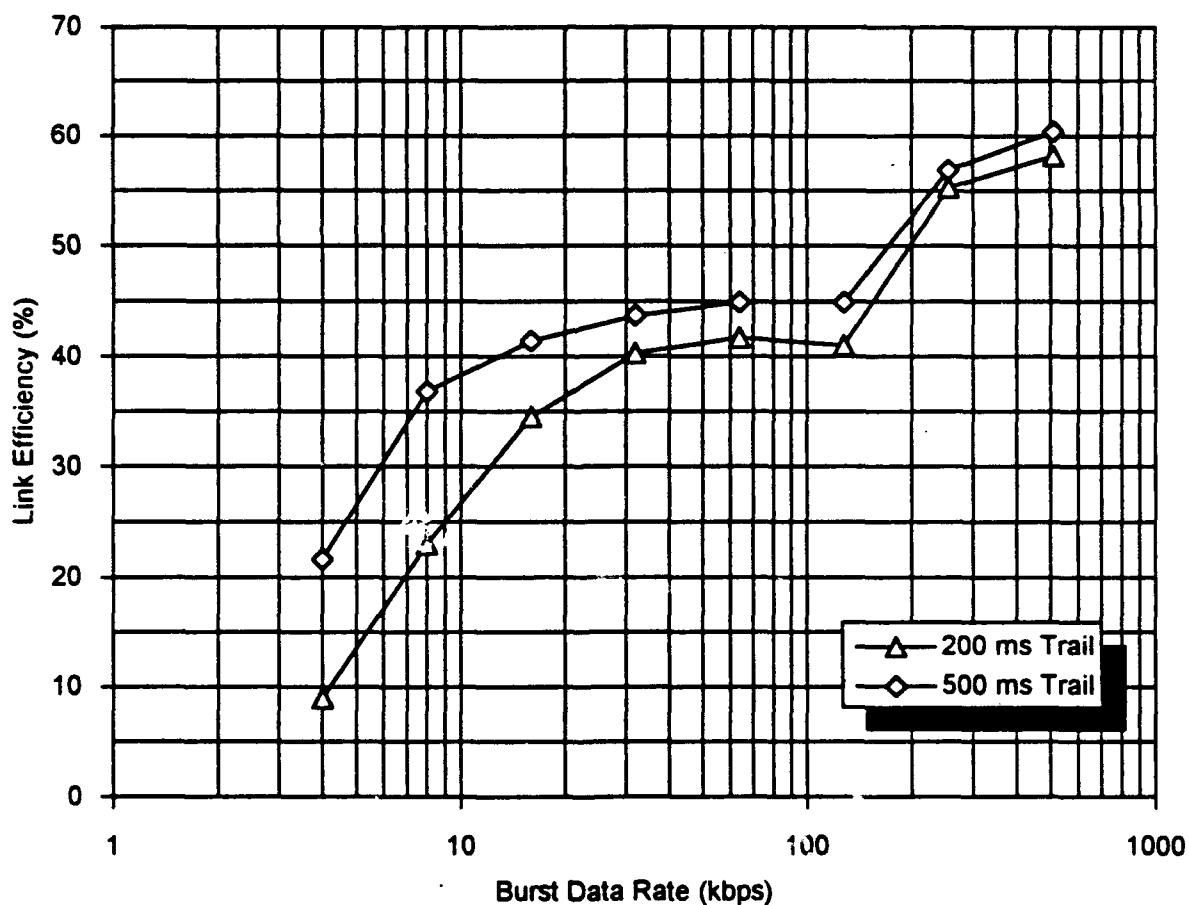


Figure 1.5-5 Link Efficiency when Operating @ an E_b/N_o of 16 dB
With the Reed-Solomon CODEC Enabled

1.6 Conclusions and Recommendations

The meteor burst modems, developed under this program, provide the capability to transmit and receive messages over a meteor burst link under a wide variety of test conditions. Burst data rate, modulator mode, and forward error control coding are operator selectable inputs. This allows the modems to be readily configured to operate at burst data rates from 4 to 512 kbps using either coherent or noncoherent modulation. Automatic data collection capability is also provided to maintain a permanent record of the time of occurrence and the duration of each meteor trail along with the amount of data received on each trail.

In addition to these existing capabilities, both the PC control terminal and the VMEbus chassis used for the modem assembly have available expansion slots that can be used for future hardware expansion. These features make the brassboard modems an ideal vehicle for developing and testing the advanced concepts needed for future meteor burst communications systems.

Recommendations for future development work are as follows:

- Additional System Tests: Most of the test conducted on the modems so far have been functional tests, which verify that the modems are functioning properly in all possible modes of operation. Additional laboratory and field tests, are needed to evaluate system performance over an operational link. The tests, planned by SAIC, are a good first step in this direction.
- Link Throughput Measurement Capability: When the modems are installed in a meteor burst link, one of the key parameters of interest is the average throughput capacity of the link. In order to test this, the modems must be able to send and receive data for an extended period of time. As the throughput capacity of the link increases, this becomes more and more difficult since the total amount of data sent over the link could be quite large. Changes in the following areas of the modem design are needed to measure the average throughput capacity of a meteor burst link:
 1. An automatic message repeat capability must be added to the modems so the same message can be sent repetitively for the entire duration of a test.

2. Receive message processing routines must be modified to maintain a record of all receive data packets and prevent those that are received more than once from being discarded.
 3. The 9.6 kbps, RS-232, interface between the modem and the control terminal must be changed to a higher speed interface so that information can be transferred from the modem to the control terminal more quickly.
 4. A RAM disk or a faster hard drive must be added to the control terminal to reduce time required to store receive data.
- Adaptive Data Rate: The data rate of the brassboard modems is controlled through direct operator intervention. This means that the modems operate at a fixed data rate irrespective of the capacity of the meteor burst link. As a follow-on effort, changes the modem hardware and software design are recommended to allow the modems to automatically adapt their data rate to match the capacity of the channel.
 - Data Compression: The addition of data compression or source coding to the brassboard modems is one method that could be used to improve the throughput performance of the meteor burst link. Data compression increase the effective throughput of the link by reducing the number of information bits required to send a message. Based on the compression ratios typically achieved using available compression techniques, a factor 2 increase in throughput is expected through the addition of data compression.

SECTION 2

SYSTEM DESIGN

2.1 Trade-Off Study

During the preliminary study phase a wide range of system parameters were considered to determine their effect on system performance. The results of this analysis and the final parameters selected for implementation in the modem design are presented in this section of the Final Report.

2.1.1 RF Parameter Selection

The effects of antenna radiation pattern, transmit power level, and burst data rate on meteor burst system performance were investigated during the study period. The results showed that for medium to long range (1000 to 2000 km) point-to-point communication links, high gain-narrow beamwidth antennas maximized throughput, minimized system delay time, and reduced susceptibility to undesired noise and interference. The study also showed that as the transmit power level and antenna gain of the system increase, the maximum burst data rate at which the system must operate in to order to achieve the full throughput potential of the link also increases.

Since antennas and the RF power amplifier weren't a part of the deliverable equipment on this contract, the remainder of the trade-off study concentrated on optimizing system performance through other system parameters such as modulation, coding, and link protocol selection.

2.1.2 Modulation

The relative performance of coherent BPSK, noncoherent DPSK, and noncoherent M-ary signaling was considered during the study phase. Since throughput is directly related to the maximum burst data rate at which the system can operate, it is desirable to choose a modulation format that can operate at the lowest possible energy per bit to noise density ratio (E_b/N_0). The BER performance of each of the modulation types considered during the trade-off study are plotted as a function of E_b/N_0 in Figure 2.1.2-1.

Of all the waveforms considered, M-ary modulation achieved the highest throughput because of its ability to operate at the lowest E_b/N_0 ratio for a given BER. For this reason, a 32-ary modulation mode was initially planned for the brassboard modems. This mode was later dropped, however, because of its complexity and the very wide channel bandwidth needed to support a given information rate. (A channel bandwidth of 1 MHz is needed to support an information rate of 80 kbps using 32-ary modulation.) In order to meet the 512 kbps information rate required for the brassboard modems, coherent BPSK and noncoherent DPSK modulation modes were chosen for the final design. These waveforms require only slightly higher E_b/N_0 than 32-ary modulation (for a BER of 10^{-2} or less) and provide an information rate of 512 kbps in a 1 MHz channel bandwidth.

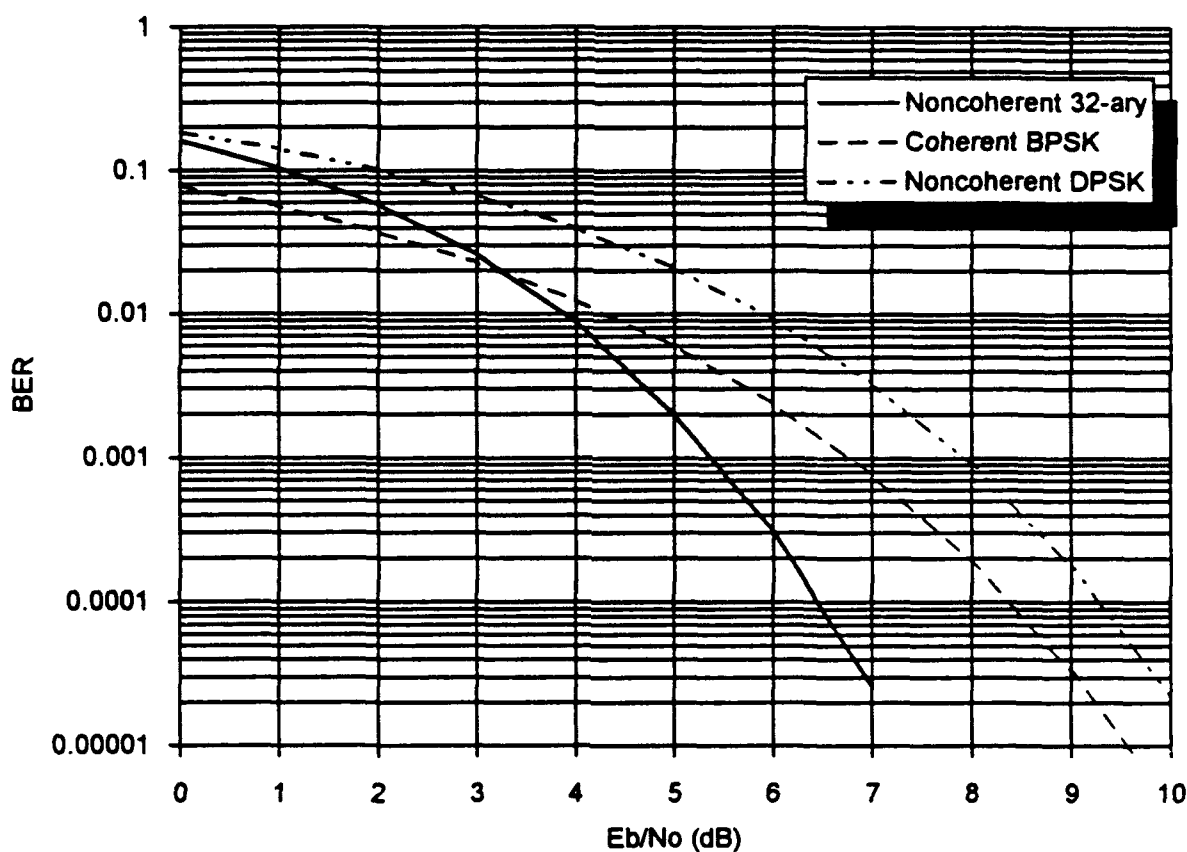


Figure 2.1.2-1 Bit Error Probability Versus E_b/N_0 for Several Modulation Formats

2.1.3 Forward Error Control (FEC) Coding

FEC coding is another way of reducing the E_b/N_0 ratio at which the system can operate. Three different forms of FEC coding were investigated during the study phase:

- Reed-Solomon (RS)
- Convolution
- Concatenated RS/Convolution

The study showed that concatenated coding would maximize the throughput for a continuous channel because of its excellent coding gain (6.7 dB at a BER of 10^{-5}). However, due to the complexity of the coding and the requirement for long trail durations to accommodate interleaving, this approach entailed high risk and therefore wasn't implemented in the modem design.

The relative performances of the two remaining coding techniques (RS and Convolutional) were found to be similar when operating in an Additive White Gaussian Noise channel (AWGN). However, the types of noise predominately seen in the lower VHF band (from 40 to 60 MHz) are manmade and atmospheric. These types of noise exhibit memory with noise occurring as random bursts. Under these conditions, RS coding is the best choice since it is less susceptible to burst errors than convolutional coding. It is also better suited to block protocols than convolutional coding. For these reasons, RS coding was selected as the best coding technique for the modem design.

Additional trade-offs, considered during the study phase, were whether to use a fixed or variable code rate system and what code rate to implement in the design. A fixed rate system is the simplest to implement because it uses a constant code rate for the entire duration of the trail. However, if the code rate is too low, too much redundancy may be present at the beginning of each trail needlessly reducing the throughput when E_b/N_0 is high and the probability of bit errors is low. On the other hand, if the code rate is too high, uncorrectable errors in the data packets can cause frequent retransmissions of data packets lowering the overall throughput of the link. A variable rate system tries to overcome this problem by adapting its code rate to match the capacity of the link as it varies over time.

During the study phase, a computer model was used to simulate the effects of link protocol on the throughput performance of a meteor burst system. The results of this investigation, which are discussed in more detail in section 2.1.4, showed that a fixed rate system with a high rate RS code provides nearly the same throughput performance as a variable rate system. The results also showed that a high rate code such as a RS(31,23) code was the best choice for the modem design. Figures 2.1.3-1 and -2 show the BER performance of the coherent BPSK and noncoherent DPSK waveforms selected for the modem design.

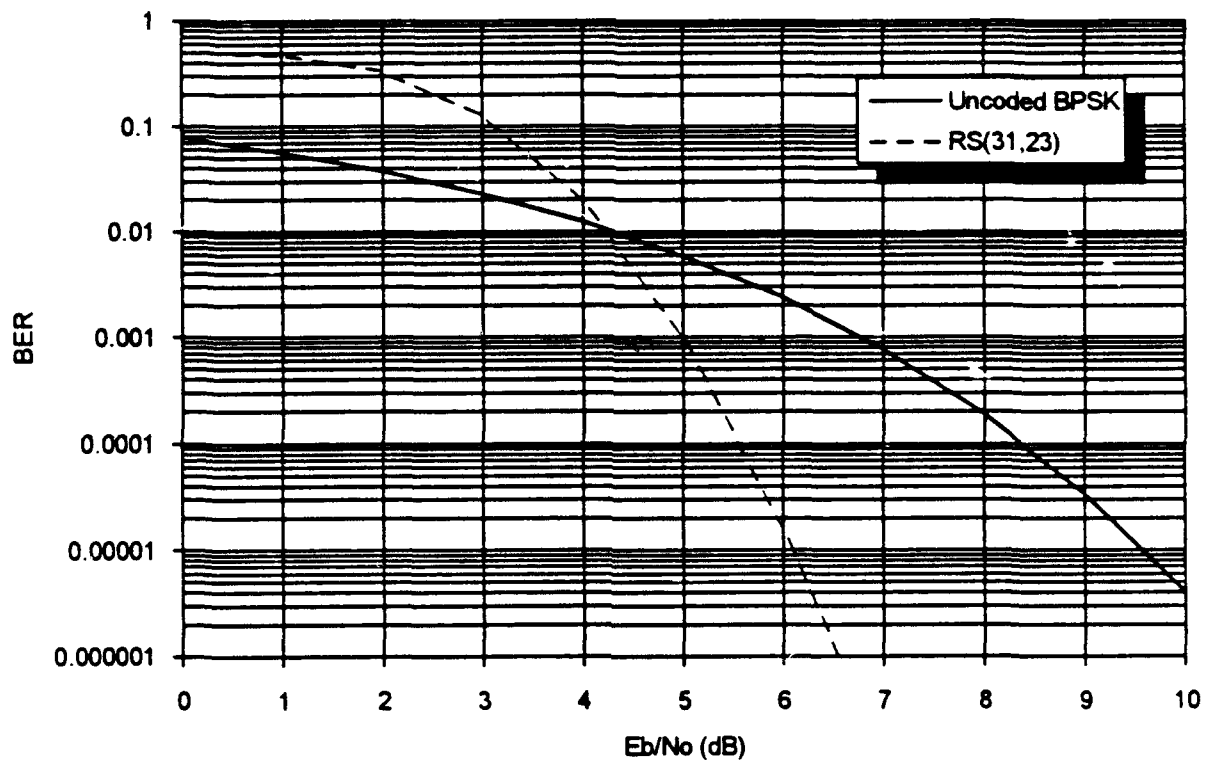


Figure 2.1.3-1 Bit Error Probability of Coherent BPSK Signaling With RS Coding

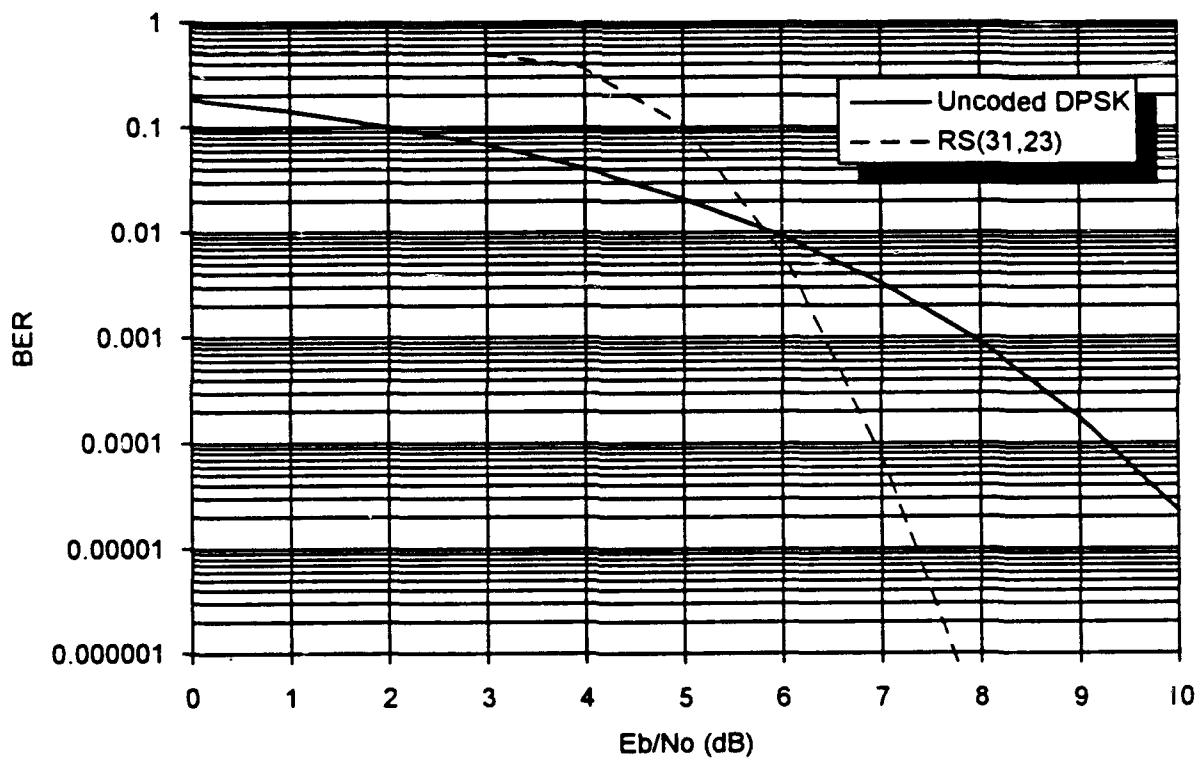


Figure 2.1.3-2 Bit Error Probability of Noncoherent DPSK Signaling With RS Coding

2.1.4 Automatic Repeat Request (ARQ) Protocols

The performance of a number of ARQ protocols for meteor burst communications was examined in conjunction with error-control codes and signaling techniques. This work was carried out by Dr. Pursley at the University of Illinois, who was a consultant on this program, during the initial 12 month study phase. The results of his investigation were described in the Design Plan [3] and were also reported in an IEEE publication [4].

The three primary types of ARQ protocols considered during the study phase were a basic ARQ, fixed-rate hybrid ARQ, and variable-rate hybrid ARQ. A brief description of each of these protocols is given in Table 2.1.4-1. Quantitative results on the effects of each of these protocols on the throughput performance of a meteor burst communication system was obtained through a link protocol computer model developed by Dr. Pursley and his research assistant at the University of Illinois.

ARQ Protocol	Description
Basic ARQ	In the basic ARQ scheme, coding is used for error detection only, no attempt is made to correct errors in the received data block. If the destination station determines that there are errors in the received block, it sends a negative acknowledgment (NACK) to the source, and the source retransmits the identical codeword.
Hybrid ARQ	A hybrid ARQ scheme employs codes that can correct errors in the received block in addition to being able to detect most commonly occurring errors. For hybrid ARQ, the destination first attempts to correct any errors in the received block. If it determines the error sequence is one that can not be corrected, then it sends a NACK to the source.
Variable Rate Hybrid ARQ	This scheme is a variation of hybrid ARQ where the code rate is tailored to match the SNR of the meteor burst communication channel. It uses a high rate code at the beginning of the trail when the SNR is high and adds more redundancy as the trail decays.

Table 2.1.4-1 Description of ARQ Protocols Investigated During the Study Phase

The results showed that a variable-rate hybrid ARQ system provided the highest throughput performance of the three protocols investigated. But the improvement over a fixed-rate hybrid ARQ system was small (10%) when operating with trail durations of 100 ms or less. Given the complexity of a variable-rate ARQ protocol and the marginal improvement in throughput that it would provide, a fixed-rate ARQ protocol was selected for the final design.

Computer simulations were also run to compare the effects of different RS code rates on the throughput performance of a meteor burst communication system. The results from this investigation are given in the Design Plan [4]. Figure 2.1.4-1 illustrates the type of effect FEC has on the throughput of a meteor burst communications system. The curves given in the figure show the maximum number of bits that could be sent over a 500 ms underdense trail plotted as a function of the peak signal-to-noise ratio of the trail. Notice that the difference in throughput provided by a 3/4 and a 7/8 rate RS code is small, so either code rate could be used in the modem design. A RS(31,23) code was selected for the final design, which was the closest to a 3/4 rate code that the RS CODEC chip used in the modem design would allow. As shown in the figure, this code should optimize performance on trails with E_b/N_0 ratios of 10 dB or less.

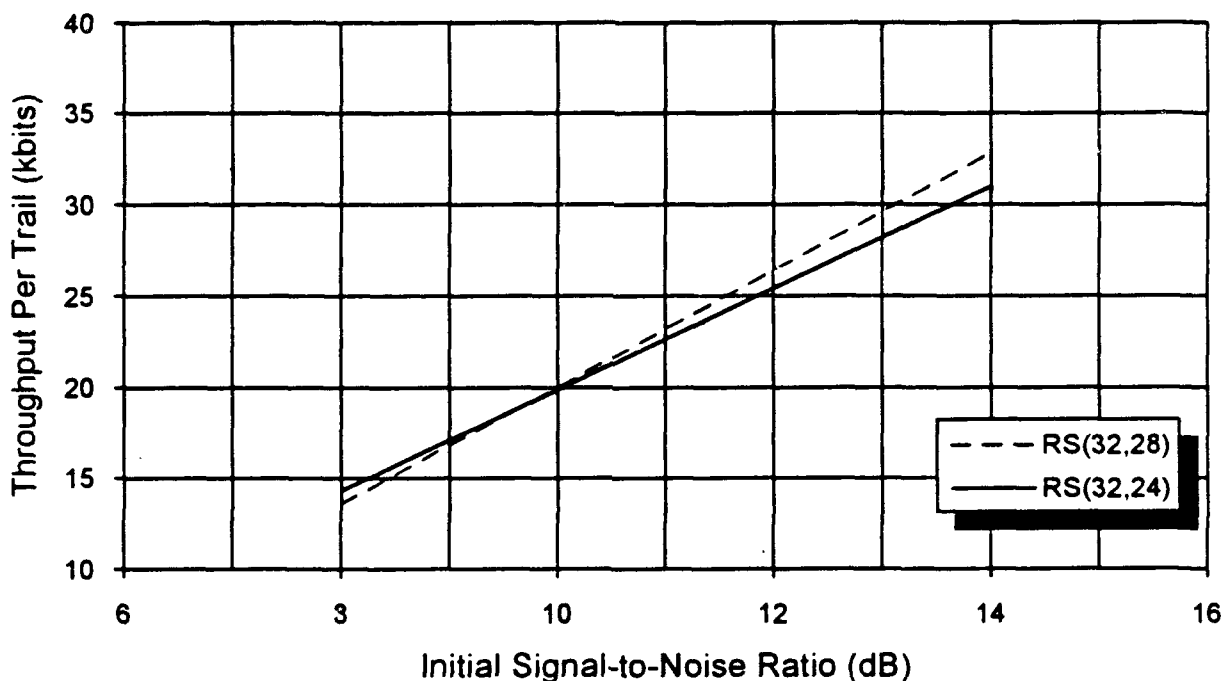


Figure 2.1.4-1 Effect of RS Code Rate on Throughput Per Trail for Fixed Rate Hybrid ARQ with BPSK Signaling and a Trail Duration of 500 ms

2.2 Link Protocol

This section of the Final Report describes the link protocol used by the modems for sending messages over a meteor burst link. The protocol is basically the same as that presented in the Design Plan with slight modifications to improve performance in certain critical areas.

Figure 2.2-1 illustrates the procedure for sending a message from station A to station B. During the initial link interrogation phase, both stations continuously transmit SYNC followed by an enquire (ENQ) control frame. The SYNC pattern is used by the receiver to detect the occurrence of a meteor burst link while the ENQ control frame identifies the transmitting station and indicates its current status. Once SYNC is detected and the receiver decodes the ENQ control frame, link acquisition begins.

The link acquisition phase ensures that both stations have acquired SYNC and established a frame of reference in the packet sequence before data exchange begins. During link acquisition, each station transmits SYNC followed by an acquire (ACQ) control frame. Included in the ACQ frame is the identification of the last consecutive data packet successfully received from the responding station on a previous meteor trail.

Once a station receives the ACQ control frame, that station is then ready to begin transmitting data packets if it has a message to send. Each data packet (except the last one) is preceded by start-of-data (SOD) control frame that defines the message number and packet number of the data packet to follow as well as the total number of data packets in the message. The last data packet in the message is preceded by an end-of-data (EOD) control frame. EOD contains the message number and packet number. Since the last data packet may not need the same number of information bits as the other data packets, the number of code words contained in the data packet is included in the EOD control frame.

In order to send at least one packet of data on each meteor trail, it is desirable to keep the packet lengths as short as possible. This is especially true, when operating at the lowest data rate where the total amount of information that can be sent over a 100 ms trail is only 400 bits. On the other hand, shorter data packets increase the overhead required to send a given amount of data and unnecessarily restricts throughput when operating at the higher data rates. The link protocol selected for the modem design resolves this problem using short packet lengths when operating at low data rates and long packet lengths when operating at high data rates.

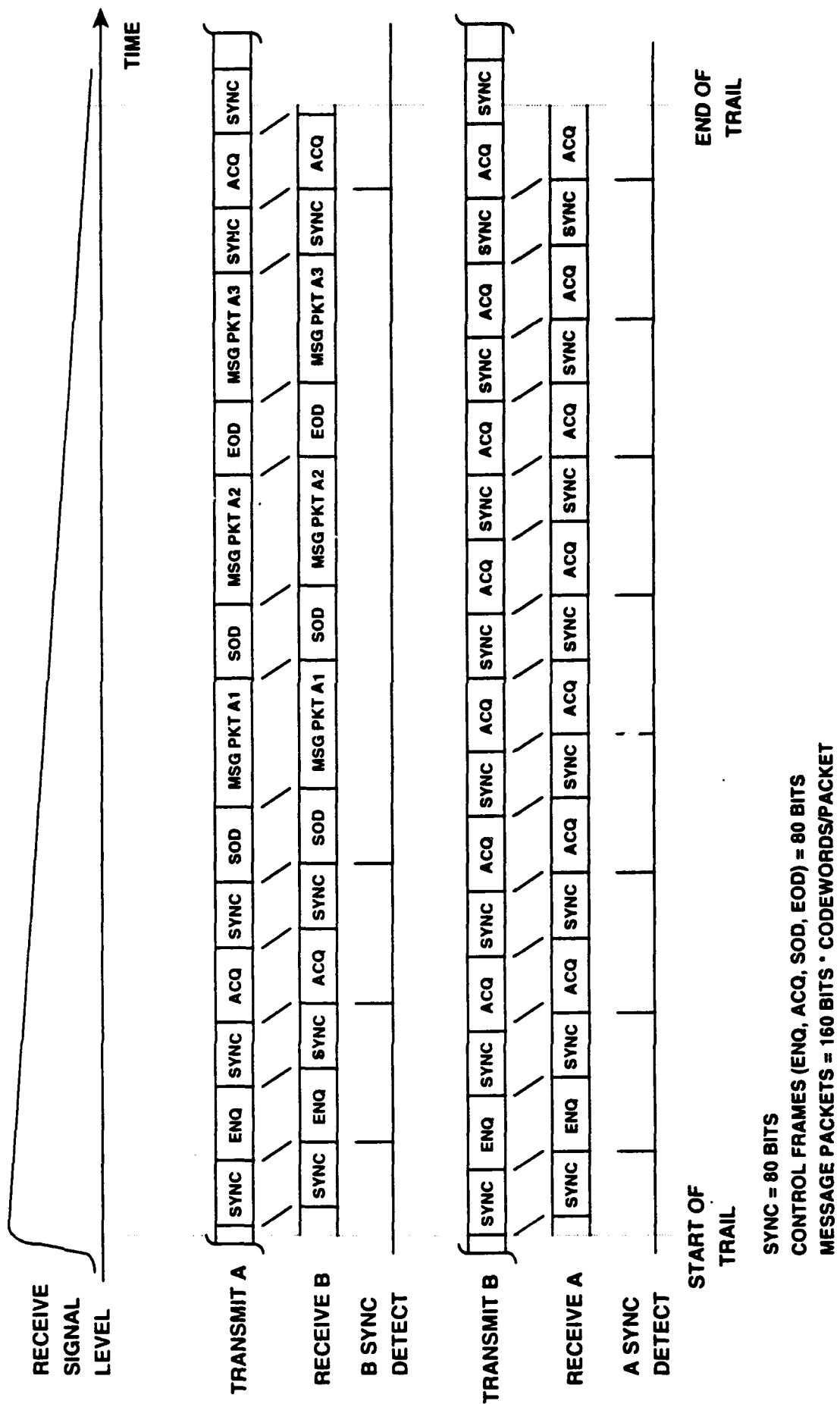


Figure 2.2-1 Link Protocol

Figure 2.2-2 shows, the format of a data packet with and without the RS CODEC enabled. Notice that the length of a data packet varies dependent on the number of RS codewords (CW) contained in a data packet. The exact number of CW's contained in a data packet and time duration of each data packet is tabulated in Table 2.2-1 as a function of burst data rate.

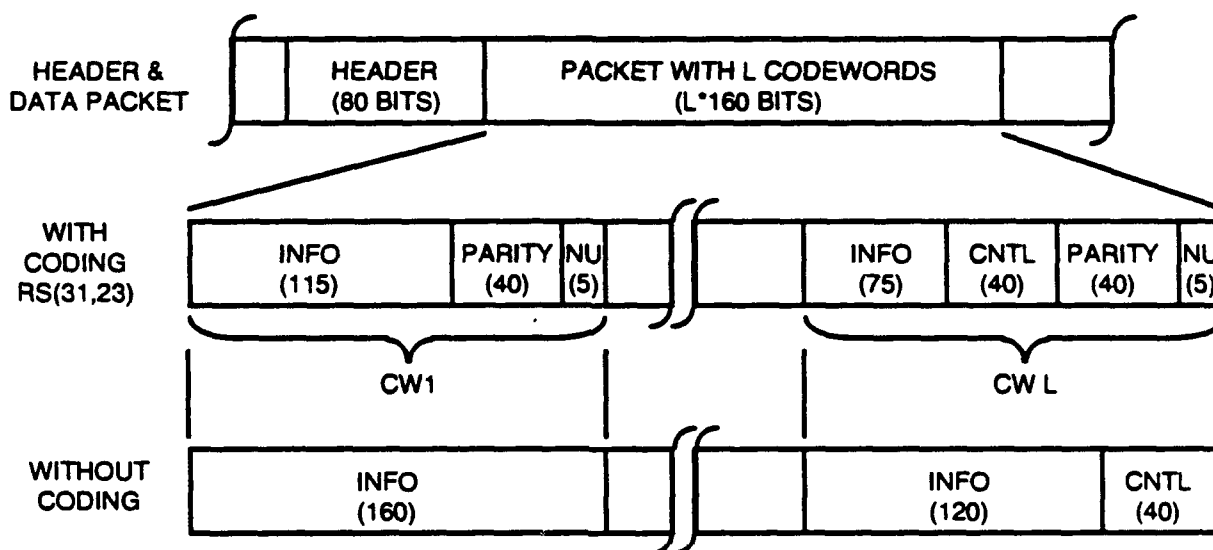


Figure 2.2-2 Format of a Data Packet With and Without the RS CODEC Enabled

Data Rate (kbps)	CW's Per Packet	Bits Per Packet	Packet Length (msec)
4	1	160	40
8	2	320	20
16	2	320	10
32	2	320	5
64	2	320	2.5
128	2	320	1.25
256	4	640	2.5
512	10	1600	3.125

Table 2.2-1 Total Number of Codewords and Data Bits Contained in Each Data Packet

The remainder of section 2.2 describes the detailed format used for each type of sync and control frame.

2.2.1 SYNC Frame

The SYNC pattern is used by the receiver to detect the occurrence of an MB link. The SYNC pattern selected for the modem is "10010000110011001100011110101110". This is a 31 bit pseudo random pattern with an extra 0 bit added to make the bit pattern divisible by 8 for byte packing.

2.2.2 Control Frame

Four basic control frames are used in the modem design; ENQ, ACQ, SOD, and EOD. Figure 2.2.2-1 shows the basic format for control frames. Each control frame is 80 bits in length and begins with a 4-bit header field, which identifies the type of control frame. Subsequent data fields contain the control frame information, a cyclic redundancy check (CRC), and RS parity bits. The CRC parity check covers the control frame information and the RS code covers both the information and CRC data fields. This allows the R-S decoder to correct errors in both the information and CRC parity check bits. The CRC check is then used to detect any uncorrectable error patterns. A 1/0 pattern is included as a buffer at the end of the control frame. Any errors in the 1/0 pattern are ignored by both the R-S and CRC decoder.

HEADER (4 BITS)	CONTROL FRAME INFORMATION (24 BITS)	CRC (16 BITS)	RS PARITY (20 BITS)	1/0 (16 BITS)
--------------------	--	------------------	------------------------	------------------

Figure 2.2.2-1 General Format For Control Frame

2.2.2.1 Enquire (ENQ)

The ENQ is transmitted by each station when probing to detect the presence of a meteor burst link. The ENQ control frame identifies the probing station and its current status. Figure 2.2.2.1-1 shows the format for an ENQ control frame.

HEADER (4 BITS)	PSID (8 BITS)	STATUS (8 BITS)	PAD (8 BITS)	CRC (16 BITS)	R-S (20 BITS)	1/0 (16 BITS)
--------------------	------------------	--------------------	-----------------	------------------	------------------	------------------

Figure 2.2.2.1-1 Format for ENQ Control Frame

The HEADER 4-bit data pattern for an ENQ control frame is 0100. The Probe Station ID (PSID) identifies the station sending the probe. Allowable ID numbers are 0 to 255. STATUS defines the status of the transmitting station. Bits 0 through 4 of the STATUS

field are reserved for sending information on the receive SNR at each particular station but are not used at this time. Bit 5 indicates whether the transmitting station has a message to send, and bit 6 indicates whether the transmitting station is busy. Bit 7 is not assigned.

2.2.2.2 Acquire (ACQ) Control Frame

The ACQ is transmitted by each station once a link is detected to acknowledge the existence of a meteor burst link. The ACQ frame identifies the last message and packet number correctly received from the responding station on a previous trail. An ACQ control frame is also transmitted whenever a link exists and the station has no data packets to send. Figure 2.2.2.2-1 shows the format for an ACQ control frame.

HEADER (4 BITS)	PSID (8 BITS)	STATUS (2 BITS)	MSG NO (6 BITS)	PKT NO (8 BITS)	CRC (16 BITS)	R-S (20 BITS)	1/O (16 BITS)
--------------------	------------------	--------------------	--------------------	--------------------	------------------	------------------	------------------

Figure 2.2.2.2-1 Format for ACQ Control Frame

The HEADER 4-bit data pattern for an ACQ control frame is 1010. The Probe Station ID (PSID) identifies the transmitting station. Allowable ID numbers are 0 to 255. The STATUS is used to define the message status of the transmitting station. This is used when the first control frame detected is an ACQ rather than an ENQ. Bit 6 indicates if the modem is busy and bit 7 indicates if the station has a message to send. The MSG NO is used to identify the message being sent. Valid message numbers are 1 to 63. The PKT NO is used to identify the packet number of the message. Packet numbers are from 0 to 255.

2.2.2.3 Start-of-data (SOD) Control Frame

SOD precedes a data packet and identifies the message and packet number for the data packet. SOD also defines the total number of data packets in the message. Figure 2.2.2.3-1 shows the format for a SOD control frame.

HEADER (4 BITS)	TOTL PKTS (8 BITS)	MSG NO (8 BITS)	PKT NO (8 BITS)	CRC (16 BITS)	R-S (20 BITS)	1/O (16 BITS)
--------------------	-----------------------	--------------------	--------------------	------------------	------------------	------------------

Figure 2.2.2.3-1 Format for SOD Control Frame

The HEADER 4-bit data pattern for an SOD control frame is 1101. The TOTL PKTS is the total number of packets in the message being sent. The number ranges from 1 to 255. MSG NO is used to identify which message number that the packet belongs to. Valid message numbers are 1 to 63. Bits 6 and 7 are 0. The PKT NO is used to identify the packet number of the message. Packet numbers are from 0 to 255.

2.2.2.4 End-of-data (EOD) Control Frame

EOD precedes a data packet and is used to indicate the end of the message. It contains the message and packet number of the last data packet. Since the last data packet doesn't always contains the same number of information bits as the other data packets, the total number of code words in the data packer are also defined in the control frame. Figure 2.2.2.4-1 shows the format for an EOD control frame.

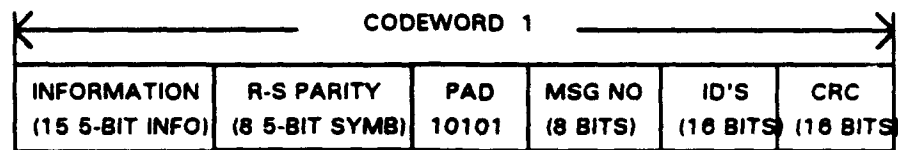
HEADER (4 BITS)	TOTL CWS (8 BITS)	MSG NO (8 BITS)	PKT NO (8 BITS)	CRC (16 BITS)	R-S (20 BITS)	1/0 (16 BITS)
--------------------	----------------------	--------------------	--------------------	------------------	------------------	------------------

Figure 2.2.2.4-1 Format for EOD Control Frame

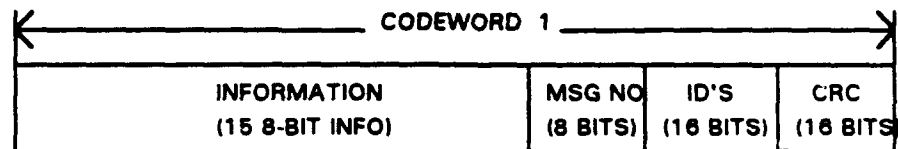
The HEADER 4-bit data pattern for a EOD control frame is 0111. The TOTL CWS is the total number of code words in the last data packet. The MSG NO is used to identify the message for which the packet is being sent. Valid message numbers are 1 to 63. Bits 6 and 7 of the MSG NO are always 0. The PKT NO is used to identify the packet number of the message. Packet numbers are from 0 to 255.

2.2.3 Data Packets

As discussed in section 2.2, data packets can consist of 1 to 10 code words depending on the data rate selected. RS encoding of the data packet is selectable by the operator. The amount of information in a code word varies depending on whether or not the RS CODEC is enabled. The formats for 1 and 2 code word data packets with and without RS coding are shown in Figures 2.2.3-1 and 2.2.3-2.

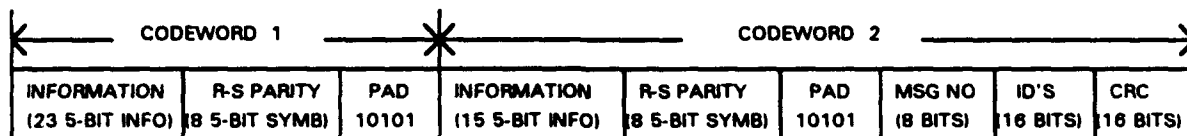


ONE CODEWORD WITH R-S

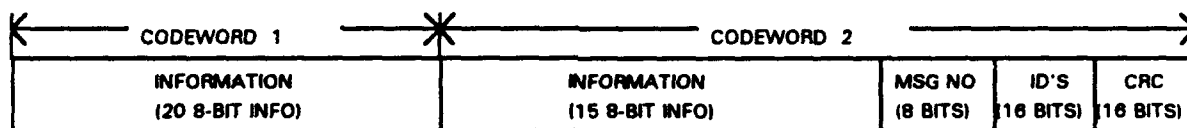


ONE CODEWORD WITHOUT R-S

Figure 2.2.3-1 Format for One Codeword Data Packet



TWO CODEWORDS WITH R-S



TWO CODEWORDS WITHOUT R-S

Figure 2.2.3-2 Format for Two Codeword Data Packet

The INFORMATION is the message data. When the RS CODEC is enabled, the information is applied to the RS encoder (5-bits at a time) where it is used to generate the 8, 5-bit, RS parity symbols. Each codeword includes a 5-bit pad, which lengthens the codeword so that it is divisible by an even number of bytes. This simplifies the processing and storage of data packets within the modem controller. When the RS CODEC is disabled, the bits normally used for RS parity are replaced with information bits, which reduces the overhead contained in each data packets but eliminates the possibility of correcting errors in the data packets at the receive end of the link.

Each codeword contains the RS parity bits needed to correct errors in the information bits contained in the codeword. The R-S Parity covers the message information as well as any message number, ID's, and CRC bits that maybe contained in the data packet.

The MSG NO is the number of the message being sent. The ID's are 8 bit in length and identify the Source and Destination station of each message. The source and destination station ID's are needed if there are more than 2 stations in a network and data packets are relayed from station to another before they reach their final destination. The CRC check covers all the INFORMATION, MSG NO, and ID's contained in all the codewords and is used to detect if there are any uncorrected errors in the complete data packet.

2.3 Control Interface Specification

A serial, RS-232, port operating at a data rate of 9.6 kbps is used as the control interface between the modem and the control terminal. The pin assignments for the control interface connector, which is located on the rear panel of the modem, are defined in Table 2.3-1.

Signal Name	Pin Designation
Shield (SHD)	1
Transmit Data (TXD)	2
Receive Data (RXD)	3
Ready to Send (RTS)	4
Clear to Send (CTS)	5
Data Set Ready (DSR)	6
Signal Ground (GND)	7, 10, 17
Data Carrier Detect (CD)	8
Data Terminal Ready (DTR)	20

Table 2.3-1 RS-232 Interface Description

Commands sent from the control terminal to the modem over the RS-232 interface, instruct the modem to select the desired transmit and receive operating frequencies, data rate, modulation type, etc. Transmit and receive ASCII data files are also transferred between the control terminal and the modem via the RS-232 interface.

A packet protocol is used for sending both control commands and data files over the RS-232 interface. The format used for the control and data packets is defined in Figure 2.3-1.

SOD	FUNCTION	LEN	DATA	CRC	EOD
(1)	(1)	(L)	(N)	(2)	(1)

() = Number of 10 bit symbols contained in each data field, where each symbol consists an 8-bit ASCII character plus a Stop and a Start bit.

Figure 2.3-1 Format for the RS-232 Data Packets

Notice that each packet contains a header (SOD, FUNCTION, LEN), a DATA field, a CRC check frame, and an End-Of-Data (EOD) frame. Since the interface is asynchronous, the symbols contained within each field are 10-bits in length, where each symbol is an 8-bit ASCII character preceded by a start-bit and followed by a stop-bit. Table 2.3-2 defines the function and data portions of the packets.

Function	Description	L	N	Data	Source
A	Transmit Frequency	1	5	#####, 5-Digit Number (kHz)	Terminal
B	Receive Frequency	1	5	#####, 5-Digit Number (kHz)	Terminal
C	Data Rate	1	1	0 = 4 kbps 1 = 8 kbps 2 = 16 kbps 3 = 32 kbps 4 = 64 kbps 5 = 128 kbps 6 = 256 kbps 7 = 512 kbps	Terminal
D	Modulation	1	1	0 = BPSK 1 = Not Used 2 = DPSK	Terminal
E	Source Address	1	3	###, 0 to 255	Terminal
F	Destination Address	1	3	###, 0 to 255	Terminal
G	Date	1	6	##, 2-Digit ASCII Month ##, 2-Digit ASCII Day ##, 2-Digit ASCII Year	Terminal
H	Time	1	6	##, 2-Digit ASCII Hour ##, 2-Digit ASCII Minute ##, 2-Digit ASCII Second	Terminal
I	Transmit Enable	1	2	##, 00 = Transmit Without Sending a Message ##, 10 = Transmit a Message ##, 10 = Stop Transmitter	Terminal
J	CODEC	1	1	0 = On, 1 = Off	Terminal
K	Parameter Request	1	1	"K"	Terminal
L	Transmit Message	4	M+4*	## Packet Number ## Total Packets M ASCII Characters	Terminal
M, N	Future Expansion	-	-	Not Used	-
O	Switch Capacitor Filter	1	1	"O" = Enable SCF	Terminal

* M = Number of ASCII characters in the packet (5120 or less)

Table 2.3-2 Serial Interface Commands

Function	Description	L	N	Data	Source
P	Self Test	1	1	"P" = Enable Self Test	Terminal
Q	BER Test	1	1	0 = TX Test, 1 = Rx Test	Terminal
R	Transmit Test	1	1	"R" = Enable TX Test	Terminal
S	Transmit Loopback Test	1	1	"S" = Enable TX Loopback Test	Terminal
T	BER Loopback Test	1	1	"T" = Enable Loopback Test	Terminal
U	Test Receive	1	1	"U" = Enable Receiver Test	Terminal
V	Reed-Solomon CODEC	1	1	0 = Enable CODEC 1 = Disable CODEC	Terminal
W	Future Expansion	-	-	Not Used	-
X	Trail Statistics	1	1	"X" = Request Statistics	Terminal
Y	Acknowledgement	1	1	Data = Function Being Acknowledged	Terminal
Z	Request Attention	1	1	"Z" = Request Attention	Modem
a	Transmit Packets	1	8	##, TX Message Number ###, TX Packet Number ###, Total Number of Packets in TX Message	Modem
b	Receive Packets	1	8	##, RX Message Number ###, RX Packet Number ###, Total Number of Packets in RX Message	Modem
c	ASCII Text Transfer	4	R*	R ASCII Characters	Modem
d	Trail Statistics	2	23	###, Trail Amplitude (dBm) #####, Trail Start Time (HH:MM:SS) #####, Trail Duration (0 - 1.999 min) #####, Bits RX Error Free ###, Noise Level (dBm)	Modem
e	Receive Message	4	R+4	##, Packet Number ##, Total Number of Packet R ASCII Characters	Modem

* R = Number of ASCII characters in the receive packet (1000 or less)

Table 2.3-2 Serial Interface Commands (Cont)

Function	Description	L	N	Data	Source
f	Parameter Response	2	40	#, Transmitting Status #####, Transmit Frequency #####, Receive Frequency ###, Data Rate #####, Modulation ###, Probing Station Addr #####, Date #####, Time ###, CODEC	Modem
g, h, i	Future Expansion	-	-	Not Used	-
j	Self Test Response	1	5	SRAM Test: 1=Pass, 0=Fail DRAM Test: 1=Pass, 0=Fail ROM Test: 1=Pass, 0=Fail RSBCH Test: 1=Pass, 0=Fail TX BB Test: 1=Pass, 0=Fail	Modem
k	BER Test Response	2	23	#, 0=TX Test, 1=RX Test "BER Error Rate Testing"	Modem
l	Transmit Test Response	2	19	"Transmitter Testing"	Modem
m	Transmit Loopback Response	2	10	#, 1=Pass, 0=Fail "Transmitter Loopback Testing"	Modem
n	BER Loopback Response	2	20	"BER Loopback Testing"	Modem
o-y	Future Expansion	-	-	Not Used	-
z	Request Initialization	1	1	1 = Request Initialization	Modem

Table 2.3-2 Serial Interface Commands (Cont)

SECTION 3

HARDWARE DESIGN

This section of the Final Report describes the modem hardware design and the performance requirements considered during the design. Problems encountered in meeting with the 512 kbps data rate requirement are discussed along with the trade-offs made to resolve these difficulties. Schematic diagrams and board layouts for each section of the modem are included in Appendix A of this report.

3.1 Control Terminal

The control terminal is an IBM PC/AT compatible computer through which the operator controls and monitors the status of the modem. The control terminal includes a standard printer interface, monitor, keyboard, 5.25" floppy disk drive (Qty 2), and a 40 Mbyte hard disk. Available memory consists of 1 Mbyte of RAM and can be expanded to 4 Mbytes using existing memory expansion sockets located on the motherboard.

The primary functions performed by the control terminal are as follows:

- Selection of the Transmit Data or Message File.
- Selection of the Transmit and Receive Data Rates (4 to 512 kbps).
- Selection of the Modulation Format (BPSK or DPSK).
- Date and Time Selection.
- Selection of the Transmit and Receive Frequency of Operation.
- Receive Messages From the Modem Controller.
- Access Disk Drives.
- Print Database Information.
- Receive and Display Message Status.

Operator interface and control of the modem is based on a menu-driven display. Upon initial power-up, the control terminal automatically displays the Main Menu shown in Figure 3.1-1, which allows the operator to select one of five submenus; Database, Parameter, Transmit, Configure, and Quit. The Database option allows the operator to edit, review, delete, or print message or statistics files. The Parameter option allows the operator to review or change the modem current operating parameters such as the transmit and receive operating frequencies or the burst data rate. Selection of the Transmit option, enables the transmitter

and allows the operator to begin sending and receiving messages. Configure allows the operator to review or change the file pathnames for the various databases. Quit causes the control terminal to exit the program and return to DOS.

At the top of the Main Menu display screen is a traffic status window where information is shown on the status of transmit and receive messages. The status window shows the identification numbers of the messages currently being received and transmitted, the total number of data packets in each message, and the number of data packets successfully completed. The Main Menu options, shown in the center of the terminal display screen, can be selected through the use of the Up/Down arrow keys on the keyboard or the 'Function Keys'. The selected mode is executed when the ENTER key is pressed. A detailed description of each menu and the procedures for operating the modem are given in the Operator's Manual [6].

Transmit Message Number.... 204	Packets Sent 5 of 10
Receive Message Number.... 63	Packets Received ... 7 of 23
<div style="border: 1px solid black; padding: 10px; text-align: center;"> MAIN MENU Database Parameter Transmit Configure Quit </div>	
10-17-1990	05:07:53
F1:HELP F2: Database F3: Parameter F4: Transmit F5: Configure F6: Quit	

Figure 3.1-1 Control Terminal Main Menu Display Screen

3.2 Modem Controller and Baseband Section

The modem controller and baseband section, shown in Figure 3.2-1, consists of three boards; a Single Board Computer (SBC), a transmit baseband board, and a receive

baseband board. The modem controller and baseband section is responsible for control of the modem and the processing of all transmit and receive baseband data.

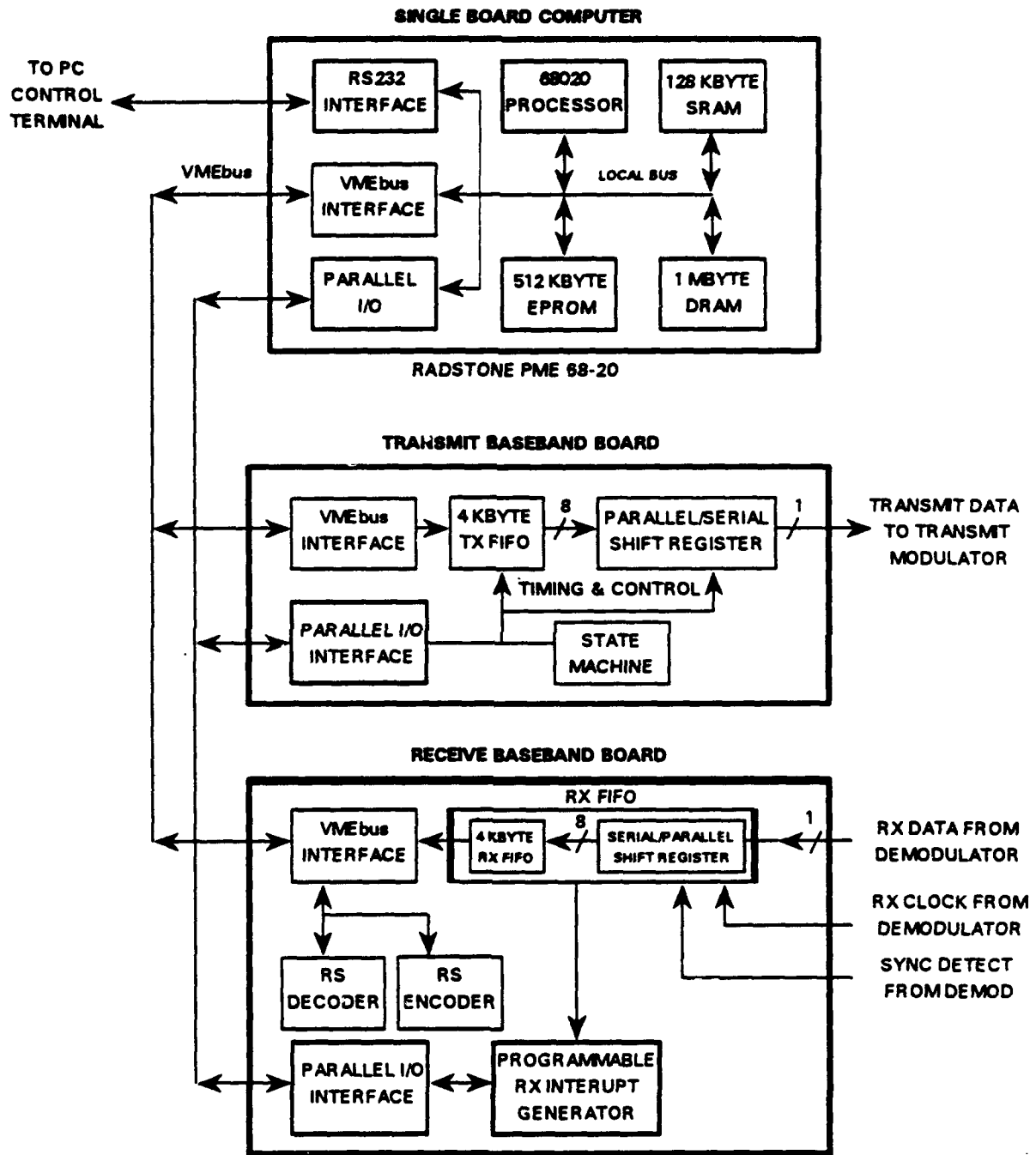


Figure 3.2-1 Block Diagram of the Modem Controller and Transmit/Receive Baseband Section

As shown in figure 3.2-1, the SBC connects to the PC control terminal through an RS-232 interface. Command information, sent from the control terminal to the modem controller over the RS-232 interface, instructs the controller to select the desired transmit and receive operating frequencies, data rate, modulation type, etc. Transmit and receive ASCII data files are also transferred between the control terminal and the modem controller via the RS-232 interface at a data rate of 9.6 kbps.

A high-speed VMEbus is used to transfer transmit and receive data between the SBC and the transmit and receive baseband boards. A parallel I/O bus provides the control interface between the SBC and the other boards in the modem. This bus has 24-lines which allow the SBC to set the frequency, modulation, data rate, enable or disable the RS CODEC, and enable or disable the transmitter.

Single Board Computer

A block diagram of the SBC computer is given in Figure 3.2-2. It consists of a high performance, VMEbus compatible, board-level computer supplied by RADSTONE TECHNOLOGY. Key features are a 32-bit, 68020 microprocessor operating at a 20 MHz (50 ns) clock rate, 1 Mbyte of dynamic RAM (DRAM), 128 kbytes of static RAM (SRAM), and 512 kbytes of EPROM.

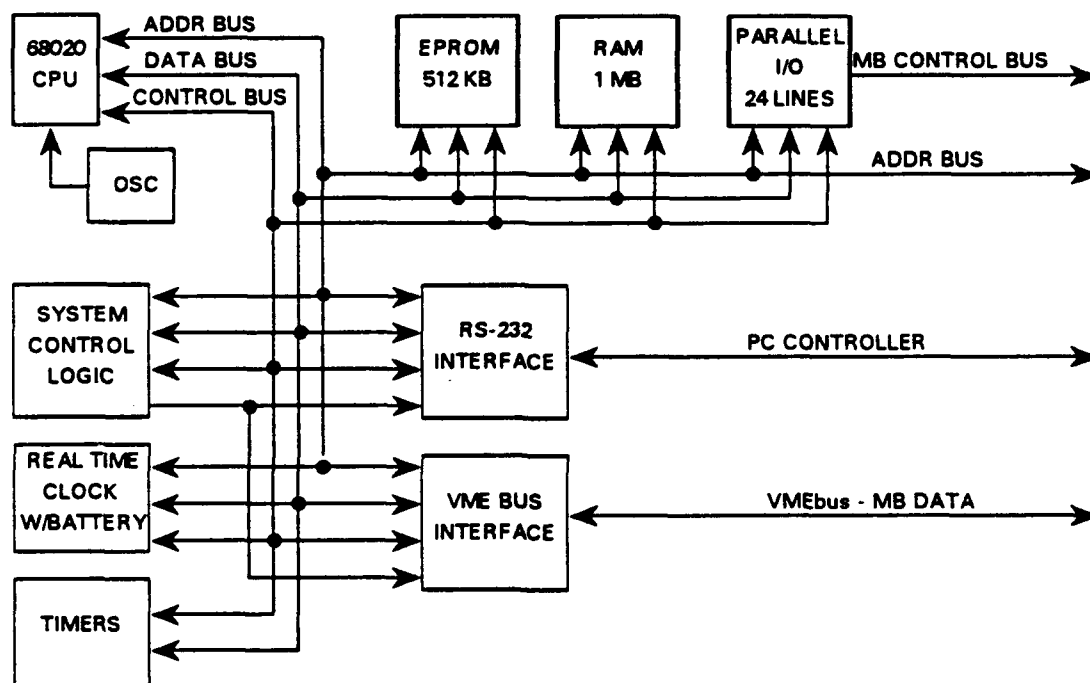


Figure 3.2-2 Single Board Computer Block Diagram

Transmit Baseband Board

A block diagram of the transmit baseband board is given in Figure 3.2-3. This board buffers the transmit data supplied by the SBC and converts it to a serial data stream for output to the transmit modulator. All data except the BPSK sync frame is differentially encoded prior to output from the transmit baseband board to eliminate the possibility of phase inversions in the receive data when operating in BPSK or DPSK mode. Differential encoding isn't needed on the sync frame since the receive correlator can detect both inverted and non-inverted sync frames

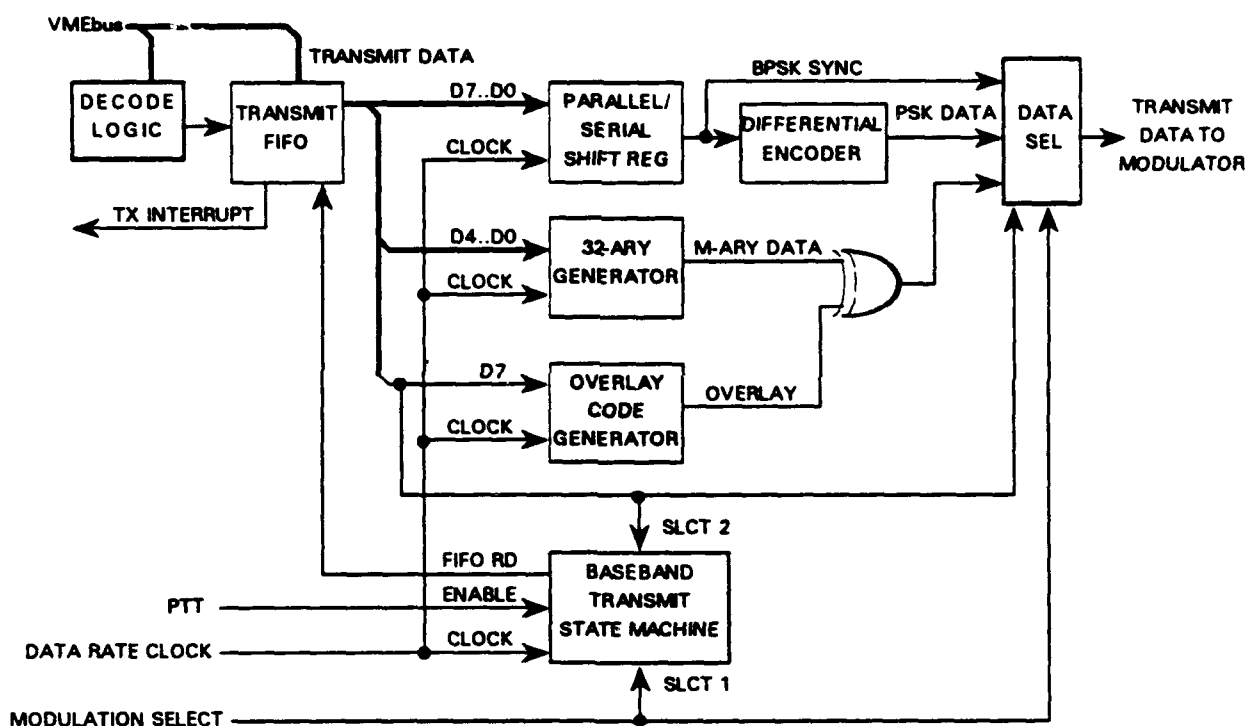


Figure 3.2-3 Block Diagram of the Transmit Baseband Board

The transmit baseband board also includes a 32-ary encoder and overlay code generator, which allows the transmit baseband data to be encoded into an M-ary modulated waveform. As discussed in section 2.1.2, this waveform was dropped from the final design because of the wide channel bandwidths needed to support a given data rate. However, the hardware was left in the modem so that it could be implemented at a later date if so desired.

Receive Baseband Board

A block diagram of the receive baseband board is given in Figure 3.2-4. This board accepts receive data from the multimode demodulator and buffers it until the data can be transferred to the SBC for further processing. The receive baseband board contains the differential decoder and receive FIFO used to decode and buffer the receive data in both BPSK and DPSK modes of operation. The receive FIFO, includes a built-in serial-to-parallel shift register, which converts the receive data to a parallel form prior to storage in the receive FIFO.

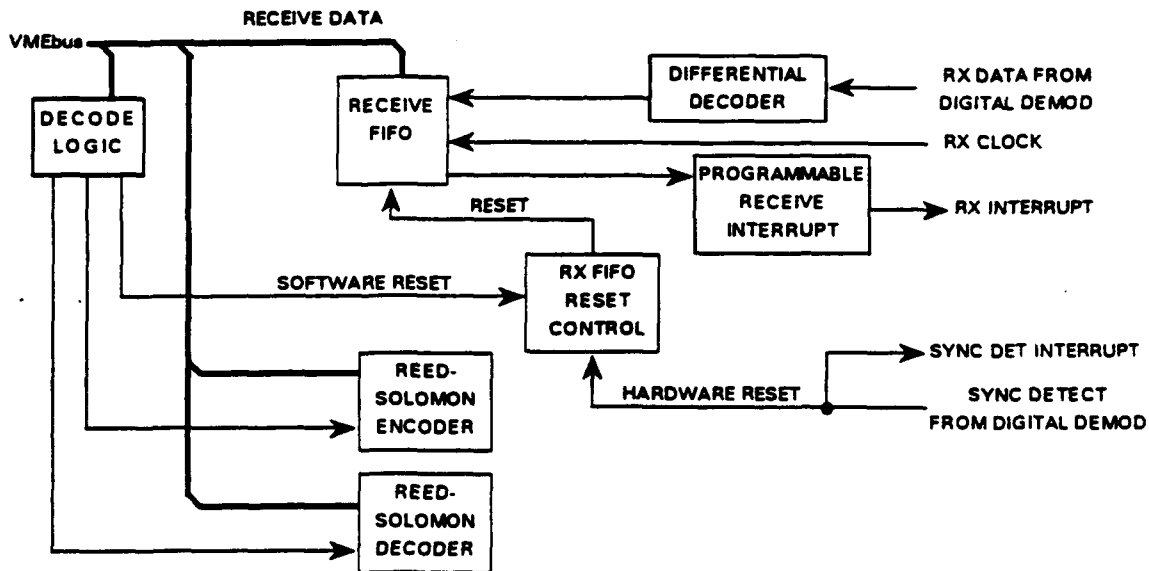


Figure 3.2-4 Block Diagram of Receive Baseband Board

The receive baseband board also houses the Reed-Solomon CODEC chips, which are used for forward error control coding (FEC) on both control frames and data packets. Separate transmit and receive CODEC chips are used to encode the transmit data and decode the receive data to minimize the processing time required for FEC coding. The CODEC selected for the modem design is a VLSI chip supplied by Thomson-CSF. The chip is programmable and can handle any RS code with a symbol size from 3 to 8 bits in length. It operates at all possible RS code rates and can encode or decode a data packet containing a single RS codeword in less than $720 \mu s$.

3.2.1 Initialization and Control

During initialization and control update periods, the following information is passed from the PC control terminal to the modem controller:

- Transmit Frequency (40 to 60 MHz)
- Receive Frequency
- Date
- Time
- Modulation (BPSK or DPSK)
- Data Rate (4 to 512 kbps)
- CODEC (On or Off)
- Source Station Address
- Destination Station Address
- Transmit Message Data

Once the SBC receives this information, it configures the modem according to the operating parameters and awaits a command from the control terminal to begin transmitting and receiving data over the meteor burst link.

3.2.2 Transmit Operation

When the SBC receives a message from the control terminal to begin transmitting, it formats and encodes the transmit message and then enables the transmitter. The transmit baseband board reacts by generating an interrupt that instructs the SBC to transfer the information to the transmit baseband board over the VMEbus. This information is loaded into a 4 kbyte transmit FIFO where it is stored until it is read out 1 byte at a time and converted to a serial bit stream. When the next to the last data byte is read out of the transmit FIFO, the SBC has 16 data rate clock cycles to begin refilling the FIFO before it runs out of data. The SBC must respond within the 16 data rate clock cycles to ensure that a continuous stream of data is always available at the output of the transmit baseband board. The timing requirements that this imposes on the modem design are described in this section and in section 3.2.4.

During the link acquisition phase, the modem must respond quickly once a SYNC frame is detected. In order to do this, the SBC can only store a small amount of data in the transmit FIFO at any time. Once this data is read out of the FIFO and transmitted over a

meteor burst link, the transmit baseband board must interrupt the SBC with a request for more data. As the data rate increases, the time between interrupts becomes shorter and shorter. Since the SBC must handle both transmit and receive operations at the same time, it must be able to load the transmit FIFO in a small fraction of the time required by the modem to transmit the information over a meteor burst link.

The time required by the SBC to transfer 1 byte of information over the VMEbus to the transmit baseband board is 200 ns (4 clock cycles). The total time required to transfer a specific amount of data over the VMEbus is tabulated in Table 3.2.2-1 along with the time it takes the modem to transmit this same information over a meteor burst link when operating at the highest data rate.

The results show that in all cases, the time required to send data over the VMEbus is far less than the time it takes to send the same information over a meteor burst link. However, the times listed in the table are the minimum times required by the hardware assuming that no interrupts occur during the VMEbus data transfer. During normal operation, additional time is required by the software algorithms to perform other operations between each byte transfer. These times vary dependent on the state of the modem when the transmit interrupt occurs.

Bytes	Total VMEbus Transfer Time (μ sec)	Meteor Burst Transmission Time *	
		(μ sec)	% of VMEbus Transfer Time
10	2.0	156	1.28
14	2.8	219	1.28
16	3.2	250	1.28
32	6.4	500	1.28
64	12.8	1000	1.28
128	25.6	2000	1.28
256	51.2	4000	1.28
512	102.4	8000	1.28

* When Operating @ a Burst Data Rate of 512 kbps

Table 3.2.2-1 VMEbus Transfer Timing

Timing measurements made on the brassboard modems during the development phase showed that the optimum amount of data to load into the transmit FIFO during link acquisition was 14 bytes. This gives the SBC adequate time to handle all the necessary transmit and receive operations and allows a single SYNC and ENQ control frame to be loaded into the transmit FIFO at one time. Once a link has been established, the amount of data stored into the transmit FIFO increases as shown in Table 3.2.2-2.

Data Rate (kbps)	Maximum Amount of Data Stored In Transmit FIFO (Bytes)	
	During Link Acquisition	Transmission of Data Packets
4	14	30
8	14	50
16	14	50
32	14	50
64	14	50
128	14	50
256	14	4000
512	14	4000

Table 3.2.2-2 Maximum Amount of Data Stored in Transmit FIFO

3.2.3 Receive Operation

While the modem is transmitting SYNC/ENQ control frames in an attempt to establish a link, the receive baseband board is searching for a SYNC frame from another station. Receive message processing begins when the correlator (which is located in the digital demodulator section) detects a SYNC pattern in the receive data and sends a sync detect to the receive baseband board. The sync detect forces the receive baseband board to reset the receive FIFO and begin loading receive data into the 4 kbyte serial-to-parallel FIFO. Once a sufficient amount of data is loaded into the FIFO, an interrupt is sent to the SBC notifying it that receive data is now available for processing. The amount of data loaded into the FIFO before an interrupt is generated is programmable and varies with data rate as shown in Table 3.2.3-1.

When the SBC detects a receive interrupt, it reads the receive data out of the FIFO over the VMEbus. The times required for the receive data transfer are the same as those shown in Table 3.2.2-1. While the SBC is reading data from the receive FIFO, new data continues to load into the receive FIFO so that no information is lost.

Burst Data Rate (kbps)	Maximum Amount of Information Stored in the Receive FIFO Between Interrupts	
	(Bytes)	(Time in ms)
4	16	32
8	16	16
16	16	8
32	16	4
64	16	2
128	16	1
256	16	0.5
512	32	0.5

Table 3.2.3-1 Amount of Information Stored in the Receive FIFO

When the link lost, the modem must be able to reinitiate the sync search process. The SBC has the ability to reset (clear) the FIFO and reset the receive process at anytime to allow for this event.

3.2.4 Interrupt Priority and Timing

When two or more interrupts occur at the same time, the modem must decide which interrupt has priority so it can service the higher priority interrupt first. Similarly, if an interrupt of higher priority occurs during the processing of an existing interrupt, the higher priority interrupt takes precedence and must be processed first. The procedure used by the modem to handle interrupts and the timing requirements that each interrupt service routine must meet are described in this section.

Table 3.2.4-1 lists the five types of interrupts that can occur and the priority assigned to each of them. When one of these interrupts occurs, normal program execution ceases and the status of the microprocessor is saved on the stack along with a return address. The interrupt generates an offset into the Interrupt Vector Table, which contains the starting

address of each of the interrupt service routine. Program execution continues at this vector address using the interrupt address and data register values retrieved from the stack. Once the interrupt service routine is completed, any address and data registers used during the interrupt are restored to the value they contained when the interrupt occurred. The program counter is also restored from the stack to the address it contained before the interrupt occurred and program execution resumes from that point.

Interrupt Type	Priority
Transmit FIFO Empty	Highest
Receive FIFO 1/8 Full	2nd Highest
Receive FIFO Full	3rd Highest
Transmit FIFO Full	4th Highest
DUART	Lowest

Table 3.2.4-1 Interrupt Priority

Since data is clocked in and out of the transmit and receive baseband boards on the rising edge of the data rate clock, transmit and receive interrupts occur shortly after the rising clock edge. If interrupts from the transmit and receive baseband boards occur at the same time, the transmit interrupt is serviced first since it has the highest priority. Once the transmit interrupt is completed, the receive interrupt can then be processed. While the receive interrupt is being serviced, the receive FIFO (which operates under hardware control) continues to load new data so that no receive data is lost.

Figure 3.2.4-1 illustrates the timing relationship between a transmit interrupt request and the time it takes the the SBC to load transmit data into the FIFO. The time denoted as T_p is the time it takes the SBC to load the transmit FIFO with a control frame or data packets. The spacing between transmit interrupts is labeled T_s .

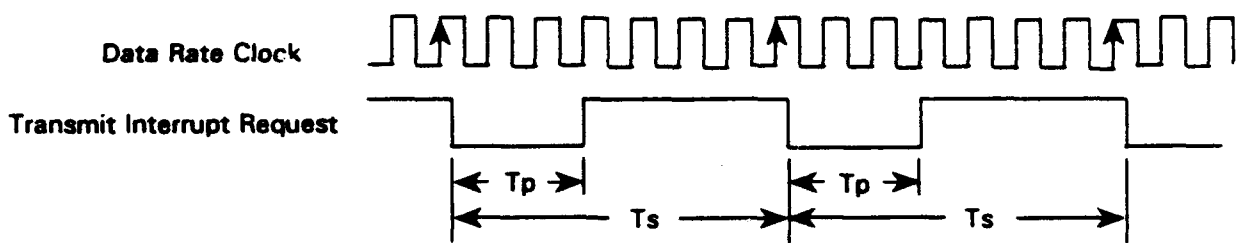


Figure 3.2.4-1 Transmit Interrupt Timing Diagram

T_p and T_s vary with data rate as shown in Tables 3.2.4-2 and 3.2.4-3. Notice that when the modem is sending control frames at a data rate of 512 kbps, transmit interrupts occur every $220\ \mu\text{s}$ and it takes the processor $70.3\ \mu\text{s}$ to load a control frame into the transmit FIFO. Similarly, when the modem is sending data packets at a data rate of 512 kbps, transmit interrupts occur every 62.5 ms and it takes the processor 11.7 ms to load the next 4 kbytes of data into the transmit FIFO. Thus the processor has sufficient time to load both control frames and data packets into the transmit FIFO between interrupts when operating at the highest data rate.

Data Rate (kbps)	Control Frame T_p (μs)		Data Packet T_p (μs)	
	min	max	min	max
4	66.4	70.3	132	146
8	66.4	70.3	197	212
16	66.4	70.3	197	212
32	66.4	70.3	197	212
64	66.4	70.3	197	212
128	66.4	70.3	197	212
256	66.4	70.3	10,890	11,715
512	66.4	70.3	10,890	11,715

Table 3.2.4-2 Transmit Interrupt Processing Time, T_p

Data Rate (kbps)	Control Frame Ts (ms)	Data Packet Ts (ms)
4	28	60
8	14	50
16	7	25
32	3.5	12.5
64	1.8	6.3
128	0.88	3.1
256	0.44	1.25
512	0.22	0.625

Table 3.2.4-3 Spacing Between Transmit Interrupts, Ts

Figure 3.2.4-2 shows the relationship between receive interrupt requests and the time required by the SBC to read and process data from the receive FIFO. In this figure, R_p denotes the time required by the processor to read and process data from the receive FIFO and R_s is the spacing between receive interrupts.

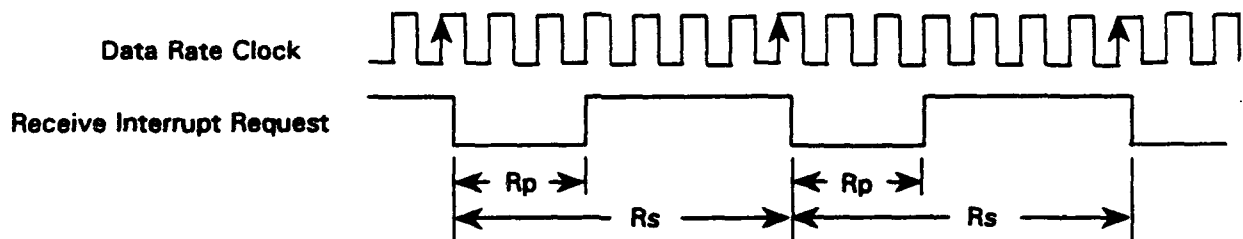


Figure 3.2.4-2 Receive Interrupt Timing Diagram

Tables 3.2.4-4 and 3.2.4-5 show how R_p and R_s vary with data rate when sending control frames or data packets. Notice that when the modem is operating at a data rate of 512 kbps, receive interrupts occur every 0.5 ms and it takes the processor 0.2 ms to transfer the 32 bytes of receive information from the receive FIFO to the SBC. At the beginning of a trail when control frames are being sent, an additional 0.7 ms is required to process each control frame. This means that the SBC can't read out and process the control frames as fast as they are received, when operating at 512 kbps. However at this data rate, control frames

are received every $219\mu s$. Since most of them are redundant, the modem doesn't need to process each control frame it receives to establish a link. Instead, the modem takes a snapshot of the receive data and then processes this data to extract the information contained in the most recently received control frame. While this is being done, the receive interrupt is disabled so that no more data will be read out of the receive FIFO until it the modem is ready to process a new control frame.

Once a link is established and the modem begins receiving data packets, the processor must read and process all receive data. Since it takes the SBC longer to process the receive information then the time between interrupts, data packets are processed off-line when operating 512 kbps. At data rates of 256 kbps or less, the SBC is able to read and process data packets faster than they are received. So at these data rates the modem decodes the receive information in real-time.

Data Rate (kbps)	Control Frame Rp		Data Packet Rp	
	Read FIFO	Process Data	Read FIFO	Process Data
4	0.1 ms	0.7 ms	0.1 ms	0.5 ms
8	0.1 ms	0.7 ms	0.1 ms	0.4 ms
16	0.1 ms	0.7 ms	0.1 ms	0.4 ms
32	0.1 ms	0.7 ms	0.1 ms	0.4 ms
64	0.1 ms	0.7 ms	0.1 ms	0.4 ms
128	0.1 ms	0.7 ms	0.1 ms	0.4 ms
256	0.1 ms	0.7 ms	0.1 ms	0.3 ms
512	0.2 ms	0.7 ms	0.2 ms	0.7 ms

Table 3.2.4-4 Receive Interrupt Processing Time, Rp

Data Rate (kbps)	Control Frame Rs (ms)	Data Packet Rs (ms)
4	32	32
8	16	16
16	8	8
32	4	4
64	2	2
128	1	1
256	0.5	0.5
512	0.5	0.5

Table 3.2.4-5 Spacing Between Receive Interrupts, Rs

The performance requirements for the multimode demodulator and the trade-offs considered in its design are described in this section of the Final Report. Table 3.3-1 lists the key performance requirements along with design goals for each item. Notice that the demodulator must be capable of receiving both coherent BPSK and noncoherent DPSK waveforms at data rates from 4 to 512 kbps. In order to meet this requirement, the demodulator must adapt its bandwidth and data rate to match that of the receive waveform. To maximize throughput over a meteor burst link, the demodulator must also provide good Bit-Error-Rate (BER) performance. A maximum BER degradation with respect to theory of 1.5 dB was selected as a design goal for both coherent and noncoherent operation.

Data Rate (kbps)	Modes of Operation	BPSK Frequency Acquisition Range	Implementation Losses	Acquisition Time (msec)	
				BPSK Mode	DPSK Mode
4	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	20 ms	19.2 ms
8	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	10.4 ms	9.6 ms
16	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	5.6 ms	4.8 ms
32	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	3.2 ms	2.4 ms
64	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	2 ms	1.2 ms
128	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	1.4 ms	0.6 ms
256	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	1.1 ms	0.3 ms
512	BPSK/DPSK	$> \pm 240$ Hz	< 1.5 dB	0.95 ms	0.15 ms

Table 3.3-1 Demodulator Performance Requirements

Two additional parameters that must be considered in the demodulator design are the bit synchronizer and carrier tracking loop acquisition times. Since a single meteor burst link typically lasts a few hundred milliseconds or less, rapid acquisition is needed to maximize the usable portion of each trail. The acquisition times shown in the table, allow 80 bit periods for the demodulator to establish bit sync in both BPSK and DPSK modes. An additional 800 μ s is allowed for carrier acquisition, when operating in BPSK mode. This additional time isn't required in DPSK mode, since the carrier tracking loop is disabled in noncoherent DPSK mode. A frequency acquisition range of greater than ± 240 Hz was selected for the carrier tracking loop in to accommodate a maximum frequency uncertainty of ± 2 PPM (parts per

million) between the transmitter and the receiver when operating in at 60 MHz. Much of the design focused on meeting these acquisition times and tracking bandwidths at all data rates.

3.3.1 Matched Filter Design

Two design approaches were considered for the demodulator matched filter design; a mixed analog/digital design and an all digital implementation. Block diagrams showing the differences between the two design approaches are given in Figure 3.3.1-1. In both cases, an input signal corrupted by noise is filtered and amplified and then applied to an integrate and dump (I&D) matched filter. The I&D filter integrates energy over a bit period of T seconds. At the end of each bit period, a decision is made on the observed waveform to decide whether the received bit was a "1" or a "0".

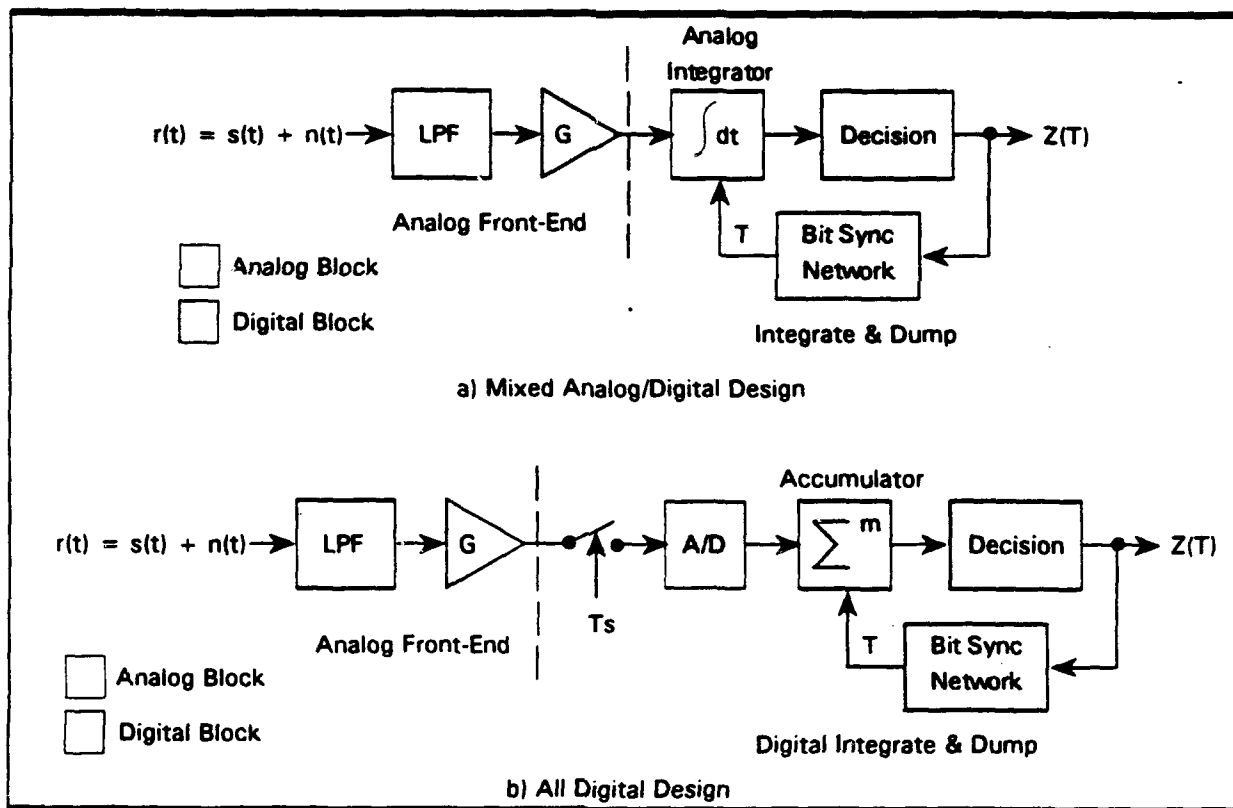


Figure 3.3.1-1 Comparison of Coherent Matched Filter Structures

After comparing the two design approaches, an all digital implementation was selected for the following reasons. First, the all digital design offers excellent performance. Chie [7] has shown that the implementation losses of a coherent digital matched filter (DMF) are less than 0.5 dB when the input signal is quantized to 4-bits of resolution and the

accumulator length, m , is greater than 4 samples per bit. Second, a DMF provides the greatest flexibility to operate over a wide range of data rates. Third, in the long run, an all digital implementation provides the greatest potential for large scale integration, with significant reductions in size and cost.

A slightly different matched filter structure, shown in Figure 3.3.1-2, is required in DPSK mode. In this mode, since the demodulator isn't phase locked to the receive signal, the signal must be split into in-phase (I) and quadrature (Q) components before it is downconverted to baseband. The I and Q components are then processed through separate I&D filters to recover the energy contained in both the I and Q components. The combined output of both I&D filters is applied to the decision circuit.

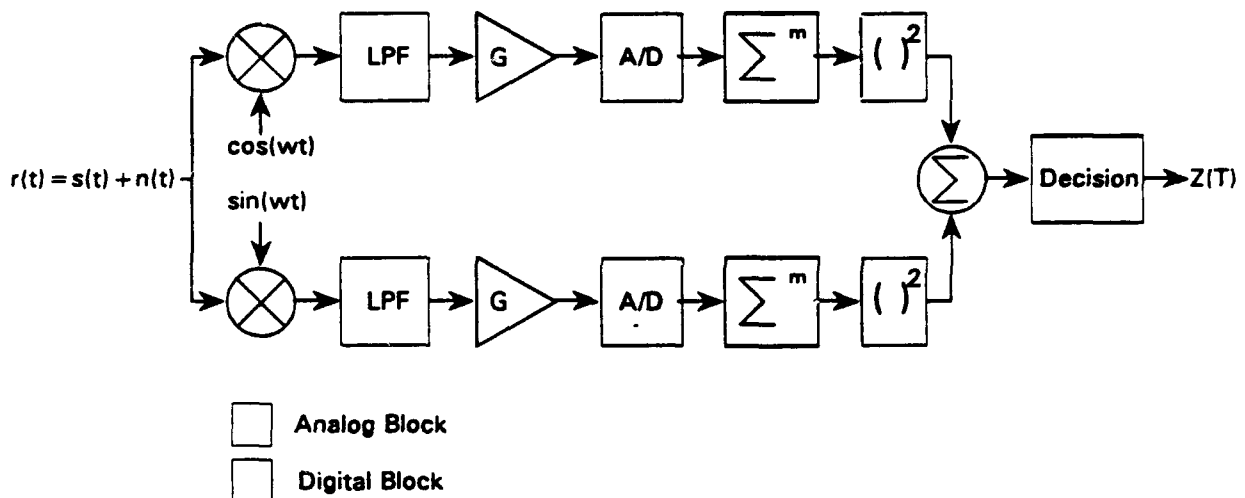


Figure 3.3.1-2 Noncoherent Digital Matched Filter Structure

Having selected an all digital implement, two basic design choices still remain between an off-the-shelf programmable digital signal processor (DSP) chip or a custom hardware design. A custom hardware design using available CMOS technology was selected for the modem design because a programmable DSP chip couldn't meet the high speed processing needed to operate at data rates of 512 kbps. The disadvantage of this approach is the complexity of a custom hardware design using standard parts. This is illustrated by the fact that each demodulator contains over 250 discrete components housed on 5 VMEbus expansion boards. However as discussed previously, the basic technology is well suited to large scale integration. And in fact, in the three years since the modem design started in 1990,

new digital signal processing components introduced by Stanford Telecom Incorporated (STI) could reduce the number of circuit boards required for the demodulator from 5 to 3 by simply taking advantage of the increased level of integration available today.

3.3.2 Demodulator Architecture

The architecture selected for the multimode demodulator provides the capability to receive coherent BPSK, non-coherent DPSK, and non-coherent M-ary modulated waveforms. In addition to multi-mode demodulation, the architecture provides a controllable matched filter structure and bit synchronizer capable of operating at data rates from 4 to 512 kbps. As shown in the block diagram of Figure 3.3.2-1, the demodulator consists of the following five functional areas:

- A/D Converter
- Phase Rotator
- Carrier Tracking Loop
- Bit Synchronizer
- Sync and M-ary Symbol Detection

A detailed description of each of the five functional areas is given in sections 3.3.2.1 through 3.3.2.5.

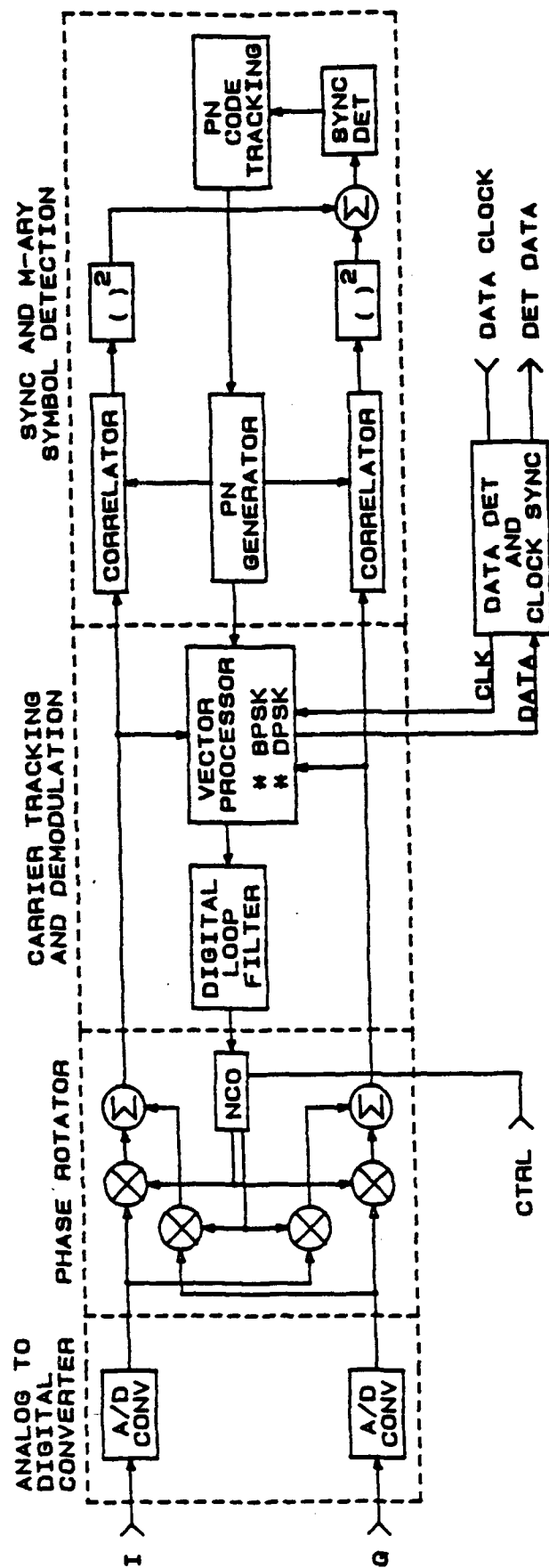


Figure 3.3.2-1 Demodulator Block Diagram

3.3.2.1 A/D Converter

A block diagram of the A/D converter section is given in Figure 3.3.2.1-1. As shown the block diagram, the analog I and Q signals are lowpass filtered in the IF module prior to output to digital demodulator. To minimize the dynamic range requirements placed on the digital matched filter, the IF bandwidth varies with data rate. Table 3.3.2.1-1 lists the combination of switchable bandpass filters and tunable lowpass filters used for each data rate. Notice that in all cases, the overall bandwidth of the IF module closely matches the data rate of the receive signal.

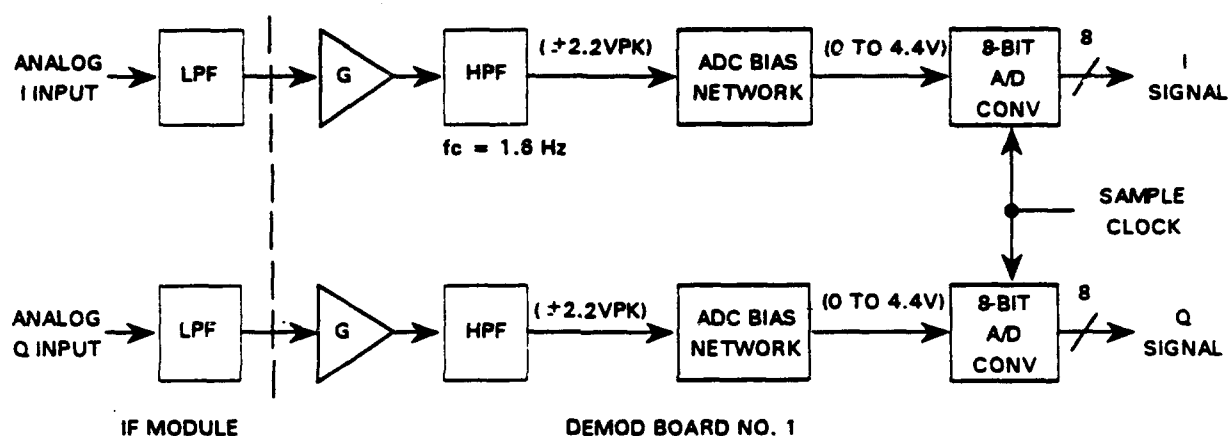


Figure 3.3.2.1-1 Block Diagram of A/D Converter Section

Data Rate (kbps)	IF Lowpass Filter		IF Bandpass Filter	Total IF BW
	3 dB BW	Filter Type	3 dB BW	3 dB BW
4	8.3 kHz	8th Order Bessel	$\pm 128 \text{ kHz}$	8.3 kHz
8	16.7 kHz	8th Order Bessel	$\pm 128 \text{ kHz}$	16.7 kHz
16	33.3 kHz	8th Order Bessel	$\pm 128 \text{ kHz}$	33.3 kHz
32	66.7 kHz	8th Order Bessel	$\pm 128 \text{ kHz}$	66.7 kHz
64	66.7 kHz	8th Order Bessel	$\pm 128 \text{ kHz}$	66.7 kHz
128	1 MHz	1-Pole Butterworth	$\pm 128 \text{ kHz}$	128 kHz
256	1 MHz	1-Pole Butterworth	$\pm 500 \text{ kHz}$	500 kHz
512	1 MHz	1-Pole Butterworth	$\pm 500 \text{ kHz}$	500 kHz

Table 3.3.2.1-1 IF Filter Bandwidth Versus Receive Data Rate

Amplification prior to the A/D converters places the I and Q signals from the IF module within the operational range of the A/D converter. Since the operational range of the A/D converter is from 0 to 4.4 volts, a DC offset is needed to place the amplified signals in the center of this range. This DC offset is provided by a combination of two elements; a highpass filter at the output of the amplifier and an A/D converter bias network.

Highpass filters, following the final analog gain stage, remove DC offsets generated by the quadrature mixer and amplifiers. A cutoff frequency of 1.6 Hz was chosen for the highpass filter to allow the demodulator to handle a data stream consisting of 20 consecutive ones or zeros with <5% tilt in the signal waveform at a 4 kbps data rate. Assuming that the data pattern is a square wave of period T, the following formula can be written for the percentage tilt [8]:

$$P = \pi \cdot F_{3dB} \cdot T \cdot 100\%$$

where P is the percentage tilt and F_{3dB} is the 3 dB bandwidth of the highpass filter. Since the maximum number of consecutive 1's or 0's for a 4 kbps data sequence is less than or equal to 20, T is equal to 10 ms. Inserting this number for T and 1.6 Hz for F_{3dB} into equation 1, results in a percentage tilt of approximately 5%.

The bias network at the output of the highpass filter injects a known DC offset into the I and Q signal paths prior to A/D conversion. Careful adjustment of this DC offset ensures that positive and negative symmetry is maintained in the digitized waveform at the output of the A/D converter.

A Mirco Power Systems, 8-bit, A/D converter (MP7684) was selected for the modem design because of its low power consumption (400 mW maximum) and high sampling rate capability (20 MHz maximum). The sampling rates used in the modem design are given in Table 3.3.2.1-2. Notice that the sampling rate varies from 128 samples/bit at the lower data rates to 8 samples/bit at the higher data rates. These sampling rates were selected to minimize transport delays that could cause instabilities in the carrier tracking loop when operating at the lower data rates. This problem is discussed in greater detail in section 3.3.2.3.

Data Rate	Sampling Rate	Samples Per Bit
4 kbps	512 kHz	128
8 kbps	1.024 MHz	128
16 kbps	2.048 MHz	128
32 kbps	256 kHz	8
64 kbps	512 kHz	8
128 kbps	1.024 MHz	8
256 kbps	2.048 MHz	8
512 kbps	4.096 MHz	8

Table 3.3.2.1-2 A/D Converter Sampling Rate Versus Date Rate

3.3.2.2 Phase Rotator

The phase rotator is a SSB frequency converter that allows coherent demodulation of BPSK modulated waveforms by eliminating any phase or frequency error in the receive signal. A complex multiplier and accumulator chip (CMAC) supplied by Stanford Telecommunications, Inc (STI) performs the phase rotator function. A block diagram of the phase rotator is given in Figure 3.3.2.2-1.

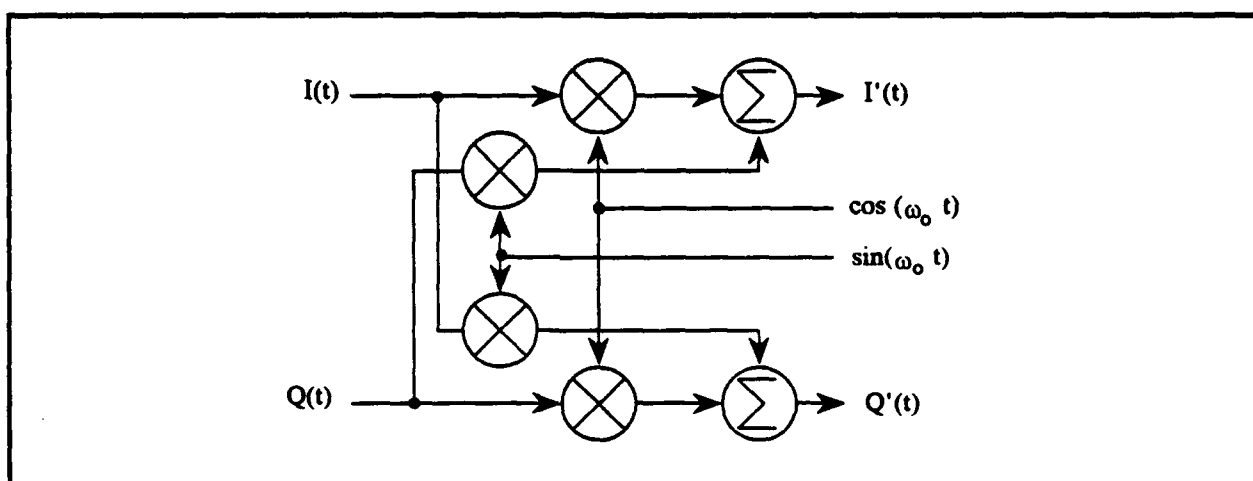


Figure 3.3.2.2-1 Phase Rotator Functional Block Diagram

The operation of the phase rotator can be expressed as follows:

$$I'(t) = I(t) \cos(\omega_0 t) + Q(t) \sin(\omega_0 t) \quad [1]$$

$$Q'(t) = Q(t) \cos(\omega_0 t) + I(t) \sin(\omega_0 t) \quad [2]$$

where: $I(t) = A(t) \cos(\omega_1 t)$ and $Q(t) = A(t) \sin(\omega_1 t)$

Substituting the above expressions for $I(t)$ and $Q(t)$ into [1] and [2] yields the following:

$$I'(t) = A(t) [\cos(\omega_1 t) \cos(\omega_0 t) + \sin(\omega_1 t) \sin(\omega_0 t)]$$

$$I'(t) = A(t) \cos[(\omega_1 - \omega_0)t]$$

$$Q'(t) = A(t) [\sin(\omega_1 t) \cos(\omega_0 t) - \cos(\omega_1 t) \sin(\omega_0 t)]$$

$$Q'(t) = A(t) \sin[(\omega_1 - \omega_0)t]$$

The results show that the phase rotator takes I and Q inputs at a frequency offset, ω_1 , and translates them to I' and Q' outputs, which are shifted in frequency by an amount, ω_0 .

3.3.2.3 Carrier Tracking Loop Design

Design of the carrier loop focused on meeting the frequency error and acquisition times defined earlier in Table 3.3-1. A block diagram of the carrier tracking loop is shown in Figure 3.3.2.3-1. The carrier tracking loop provides coherent detection of bi-phase modulated signals by mixing the baseband signals from the IF module with a local oscillator phase locked to the receive signal. This mixing action translates the in-phase (I) and quadrature (Q) signals to dc and eliminates any phase and frequency offsets in the receive signal prior to detection in the integrate and dump matched filter.

As shown in Figure 3.3.2.3-1, the phase rotator generates I and Q signals whose phase is equal to the difference between the input signal and the local oscillator I and Q reference signals. The phase rotator output signals are filtered by a half bit integrate and dump to improve the signal-to-noise ratio (SNR). The I and Q signals out of the integrate and dump circuits are applied to the bit sync and clock recovery circuits as well as the phase detector, where they are used to generate the control signal for the carrier loop.

Ideally, one would like to integrate over a full bit; however, during acquisition this isn't possible because the bit synchronizer is not synchronized. If the bit synchronizer (bit sync) timing was such that one integrated across half of the present and past bits, the output signal would be zero for a full bit period if these bits were different. This condition would leave no information to control the carrier loop. By integrating over half a bit, this condition never occurs. Under worst case timing conditions, when the past and present bit are different, no information is sent to the carrier loop for half a bit period. However, during the other half of the bit, information is available for the carrier tracking loop.

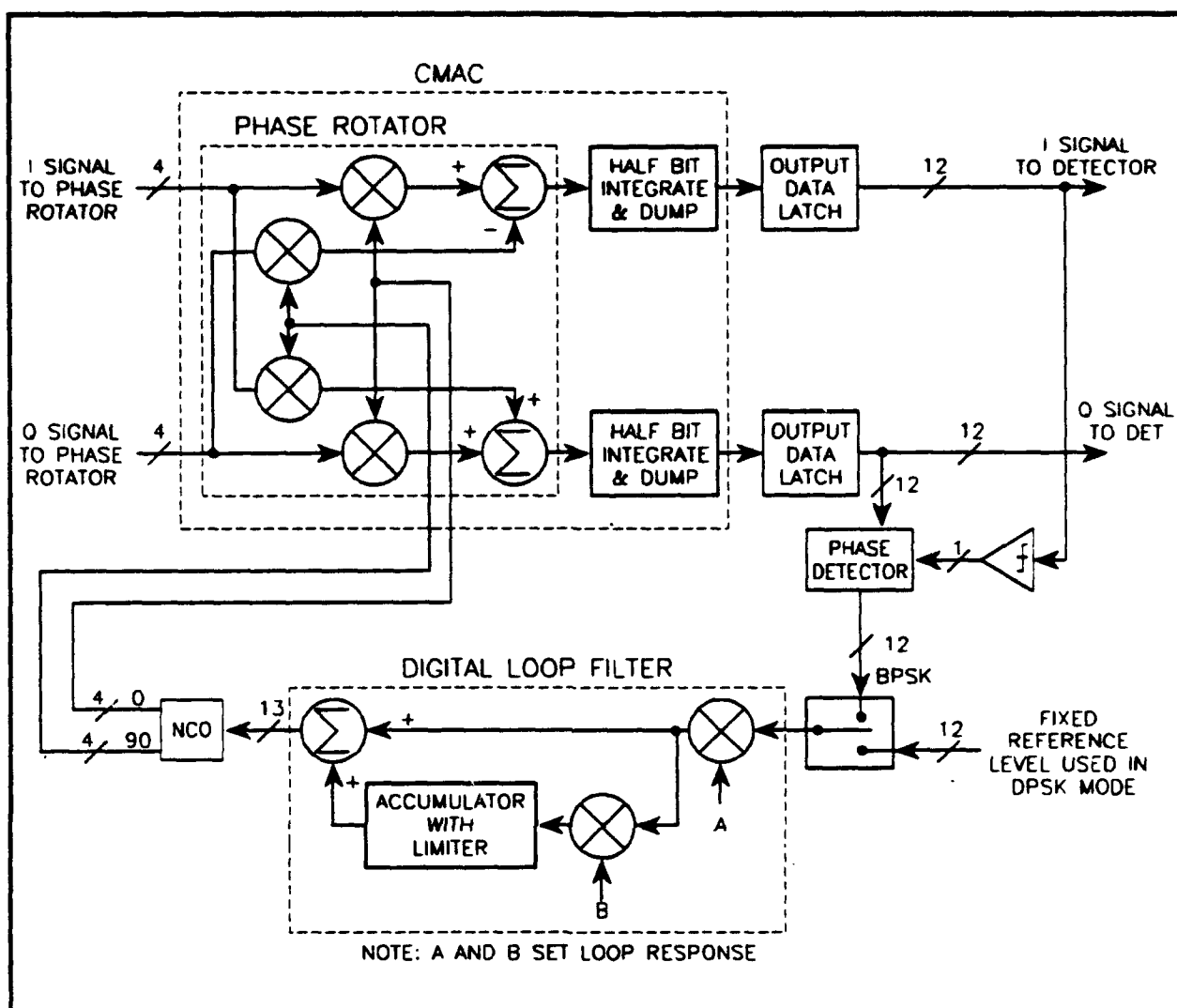


Figure 3.3.2.3-1 Carrier Tracking Loop Block Diagram

The phase rotator and integrate and dump functions are provided by a Stanford Telecommunications, Inc. (STI) complex multiplier/accumulator (CMAC) chip. The part number of this device is STI-2003. This part was selected for its ability to operate at sample rates up to 6 MSPS and the high level of integration it provides. At the time the design started, back in 1990, no other chip offered this much capability in a single device.

In DPSK mode, the carrier tracking loop is disabled and only the integrate and dump operation is used. This is accomplished by setting the numerically controlled oscillator (NCO) to a 0 Hz output frequency. This results in the I and Q reference signals out of the NCO being set at 1 and 0 respectively. In this condition, the phase rotator become transparent and I and Q output signals from the phase rotator are equal to the respective input I and Q inputs.

Phase Detector

A Costas loop with hard-limiting on the I channel is used for carrier synchronization. Hard-limiting allows a chopper multiplier to be used as the phase detector for the carrier loop, which offers the following advantages over a conventional multiplier:

- High gain on the unstable lock points
- Less gain sensitivity to signal level
- Easier to implement

The phase detector, transfer functions for a chopper and conventional multiplier are derived in Figure 3.3.2.3-2. In this diagram, θ_e is the phase error between the NCO and the receive signal. The results show, that the output from the chopper multiplier is proportional to the sine of the phase error, while the output from the conventional multiplier is proportional to the sine squared of the phase error.

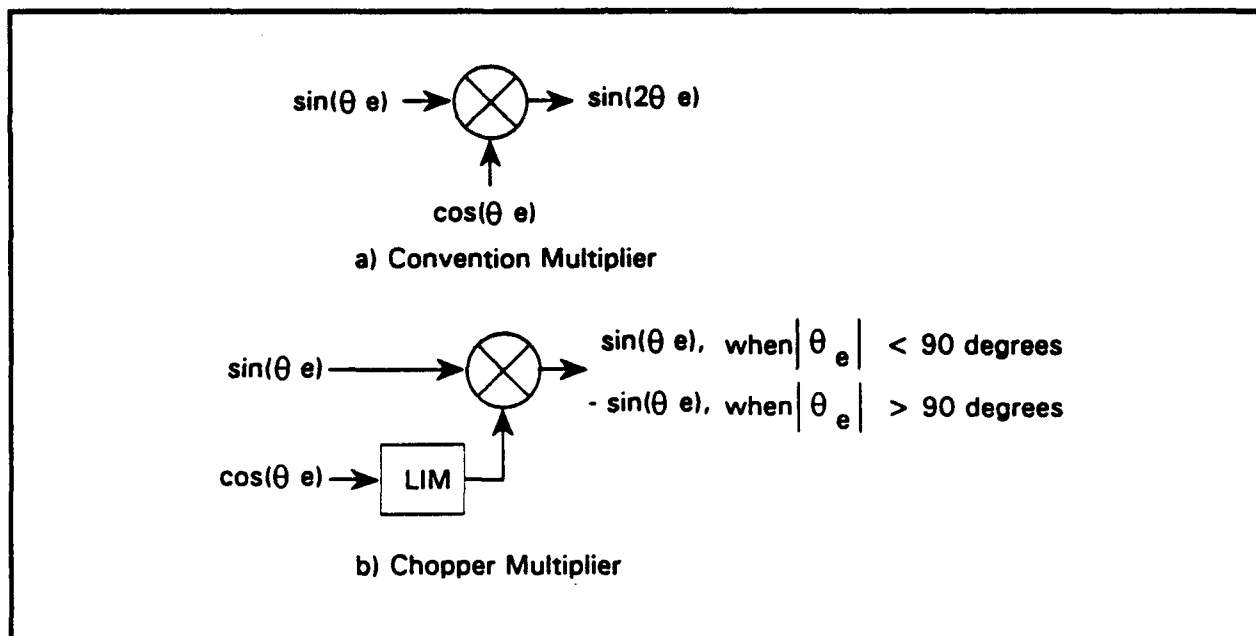


Figure 3.3.2.3-2 Phase Detector Transfer Function for Two Types of Multipliers

S-curves for a chopper and conventional multiplier are given in Figure 3.3.2.3-3. High gain on the unstable lock points at ± 90 degrees for the chopper multiplier is easily seen. This high gain reduces the acquisition time when the initial phase is close to the unstable lock point. Since the gain of the S-curve is directly proportional to the amplitude of the input signal for the chopper multiplier and the amplitude squared for the conventional multiplier, the

chopper multiplier is less sensitive to amplitude variations. This lower amplitude sensitivity of the chopper multiplier results in less variation in loop bandwidth as the input signal level changes.

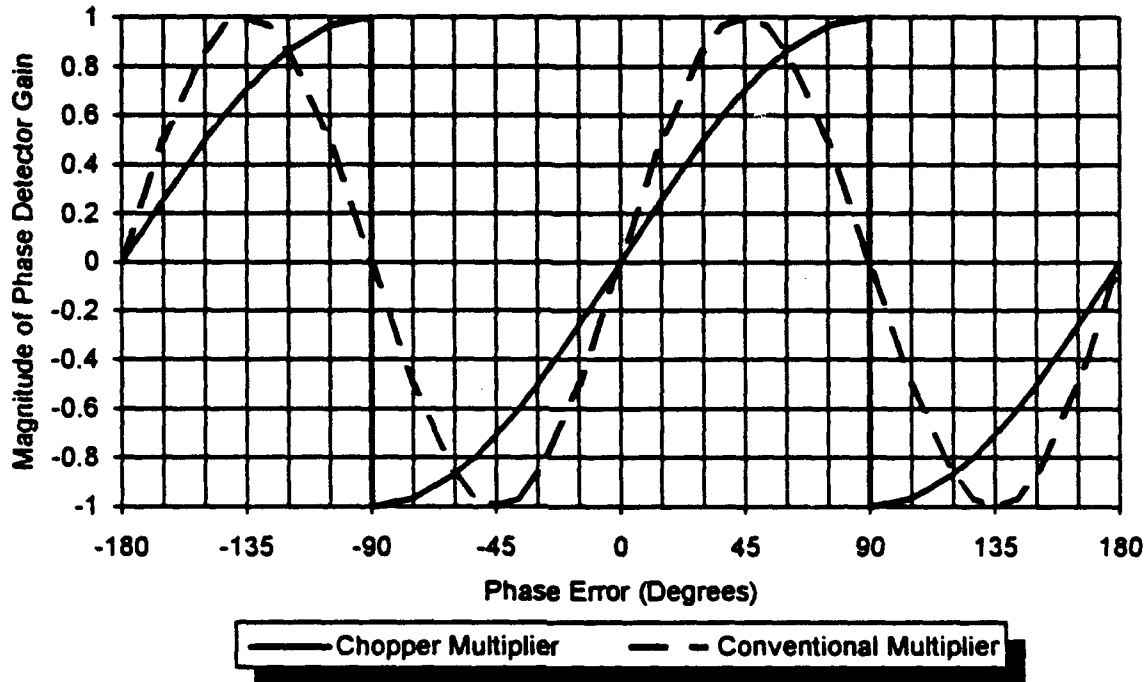


Figure 3.3.2.3-3 Comparison of S-Curves for Different Multipliers

Since the chopper multiplier requires only the sign of the I signal, it can be easily implemented using only a bank of exclusive-or gates (one for each significant bit). A conventional digital multiplier, on the other hand, is much more difficult to implement, requiring either an EPROM or a digital multiplier.

The gain of the phase detector (in volts/radian) is determined by the input signal amplitude, the number of accumulations per half bit, and the shifting down (truncating) of the digital I and Q signal out of the integrate and dump. The CMAC part used has a 22-bit accumulator, which provides adequate range for all the different data rates. The accumulator output range, accumulator rate, number of accumulations per half bit, and the number of bit shifts used for each data rate is given in Table 3.3.2.3-1.

Using these parameters, the gain of the phase detector, K_D , can be calculated as follows:

$$K_D = \frac{112.5 \cdot \pi \cdot K_A \cdot n_A}{2^{n_B}}$$

where K_A = Signal reduction from full A/D converter range
 n_A = Number of bit accumulations
 n_B = Number of bit shifts

Data Rate (kbps)	Accumulator Range	Accumulator Rate	Number of Accumulations	Number of Bit Shifts
4	2^6 to 2^{14}	512 kHz	64	4
8	2^6 to 2^{14}	1.024 MHz	64	4
16	2^6 to 2^{14}	2.048 MHz	64	4
32	2^0 to 2^{10}	256 kHz	4	0
64	2^0 to 2^{10}	512 kHz	4	0
128	2^0 to 2^{10}	1.024 MHz	4	0
256	2^0 to 2^{10}	2.048 MHz	4	0
512	2^0 to 2^{10}	4.096 MHz	4	0

Table 3.3.2.3-1 Accumulator Parameters Versus Data Rate

Numerically Controlled Oscillator (NCO)

A numerically controlled oscillator (NCO) is used to generate the I and Q reference signals for phase rotator. The NCO selected for the brassboard design is a custom CMOS LSI, which was developed by ITT-A/CD under a previous IR&D program. A block diagram of the NCO, given in Figure 3.3.2.3-4, shows that the NCO contains a 16-bit phase accumulator and a pair of ROM look-up tables. The look-up tables translate the phase accumulator output to the sine and cosine values that correspond to a particular phase.

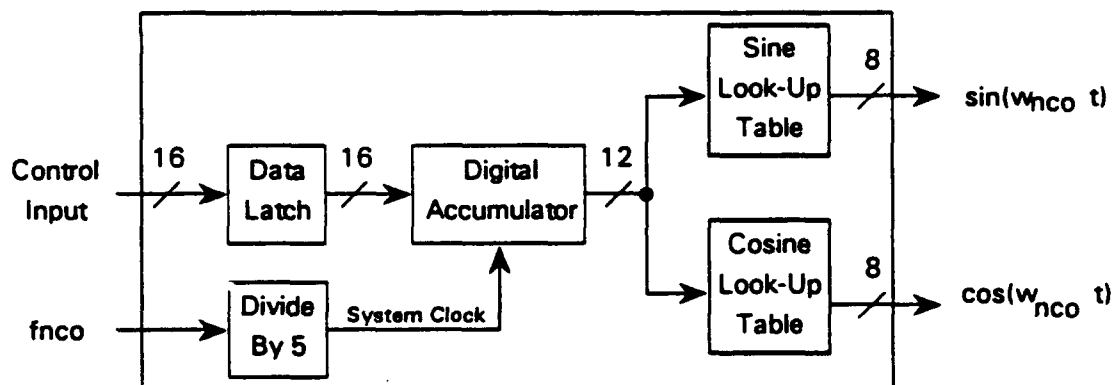


Figure 3.3.2.3-4 NCO Functional Block Diagram

The control input to NCO comes from the digital loop filter. The gain of the NCO, K_{NCO} , (in Radians/Volt Sec) is given by the following relationship:

$$K_{NCO} = \frac{2 \cdot \pi \cdot f_{NCO}}{5 \cdot 2^N}$$

where f_{NCO} = NCO clock rate
 N = Accumulator Length = 16

The NCO clock rate used for each data rate is given in Table 3.3.2.3-2 along with the NCO gain of that these clock rates provide.

Data Rate (kbps)	NCO Clock Rate (f_{NCO})	NCO Gain, K_{NCO} (Radian/Volt Sec)
4	512 kHz	$2\pi \cdot (1.5625)$
8	512 kHz	$2\pi \cdot (1.5625)$
16	512 kHz	$2\pi \cdot (1.5625)$
32	512 kHz	$2\pi \cdot (1.5625)$
64	512 kHz	$2\pi \cdot (1.5625)$
128	512 kHz	$2\pi \cdot (1.5625)$
256	1.024 MHz	$2\pi \cdot (3.125)$
512	2.048 MHz	$2\pi \cdot (6.25)$

Table 3.3.2.3-2 NCO Gain Versus Data Rate

Digital Loop Filter

A second order loop was selected for the demodulator carrier tracking to prevent cycle slips when operating at low data rates. Tausworther [9] has shown that the mean time between cycle slips depends on phase offset, loop damping factor, and SNR. Using the method presented in his paper, the mean time between cycle slips for a first order loop can be calculated. The results show that with a single-sided noise bandwidth of 400 Hz and an offset frequency of 100 Hz, the mean time to the first cycle slip is only 2.9 seconds when operating at a data rate of 4 kbps and an E_b/N_0 of 6 dB. The mean time between cycle slips is significantly improved by going to a second order loop because the phase error caused by a frequency offset is zero for a perfect second order loop.

A second order loop was achieved by placing an accumulator in the feedback path of the carrier tracking loop, as shown in Figure 3.3.2.3-1. To prevent overflow or underflow in the accumulator, the output signal range of the accumulator must be limited. This limiting is achieved by comparing the accumulator past output with the present input. If the accumulator output is at its maximum value with a positive input, the accumulator is held at the maximum value. In this state, the accumulator output only changes when a negative input is applied. This same technique is used to limit the minimum value stored in the accumulator. Selection of the limiting level determines the closed loop bandwidth.

The loop filter transfer function is controlled by two multiplication parameters, A and B. The relationship between these parameters and the closed loop response is defined in Figure 3.3.2.3-5.

Measured Test Results

The following parameters were measured on the carrier tracking loop to verify that it meets the performance requirements specified in Table 3.3-1:

- Closed Loop Frequency Response
- Frequency Acquisition Range
- Acquisition Time

The demodulator uses three different loop bandwidths to cover all data rates from 4 to 512 kbps. The closed loop response for each of these bandwidths was measured by applying a frequency modulated carrier to the I and Q inputs of carrier tracking loop and

observing the relative amplitude of the control signal at the numerically controlled oscillator. For a given set of filter parameters, slight differences in the closed loop response occur due to changes in loop transport delay when operating at different data rates. A fourth measurement, taken at 16 kbps, illustrates this fact. All four measurements were made with an input signal level of 1.5 volts peak-to-peak.

Let $H(s)$ be the closed loop response, then

$$H(s) = \frac{2 \cdot \rho \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \rho \cdot \omega_n \cdot s + \omega_n^2},$$

where ω_n = the natural frequency
 ρ = the closed loop damping factor

It can be shown that the closed loop response of the carrier tracking loop is given by the following expression:

$$H(s) = \frac{K_o \cdot K_D \cdot A \cdot s + K_o \cdot K_D \cdot f_A \cdot B}{s^2 + K_o \cdot K_D \cdot A \cdot s + K_o \cdot K_D \cdot f_A \cdot B}$$

where K_o = the NCO gain
 K_D = the phase detector gain
 f_A = the accumulator clock rate
 A & B = loop filter multiplication factors

A comparison of the two expressions shows that:

$$\omega_n = \sqrt{K_o \cdot K_D \cdot f_A \cdot B}$$

$$\rho = \frac{K_o \cdot K_D \cdot A}{2 \cdot \omega_n}$$

Figure 3.3.2.3-5 Relationship Between Closed Loop Response and Loop Filter Transfer Function

Figure 3.3.2.3-6 shows the closed loop frequency response when operating at data rates greater than 128 kbps. This data was measured with the demodulator operating at 512 kbps and shows that the loop has a 3 dB bandwidth of 1.2 kHz at this data rate.

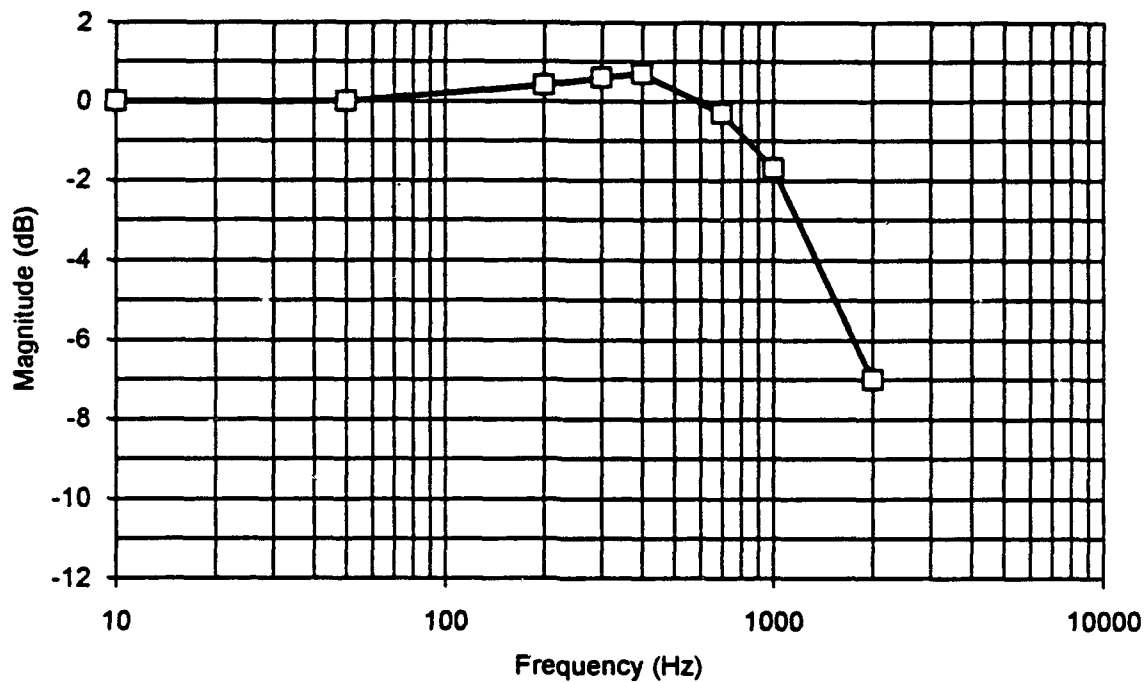


Figure 3.3.2.3-6 Closed Loop Response for the Carrier Loop at 256 and 512 kbps

Figure 3.3.2.3-7 gives the closed loop response for the 32, 64, and 128 kbps data rates. This data was measured with the modem operating at 64 kbps and shows that the loop has a 3 dB bandwidth of 680 Hz and less than 2 dB of peaking within the passband.

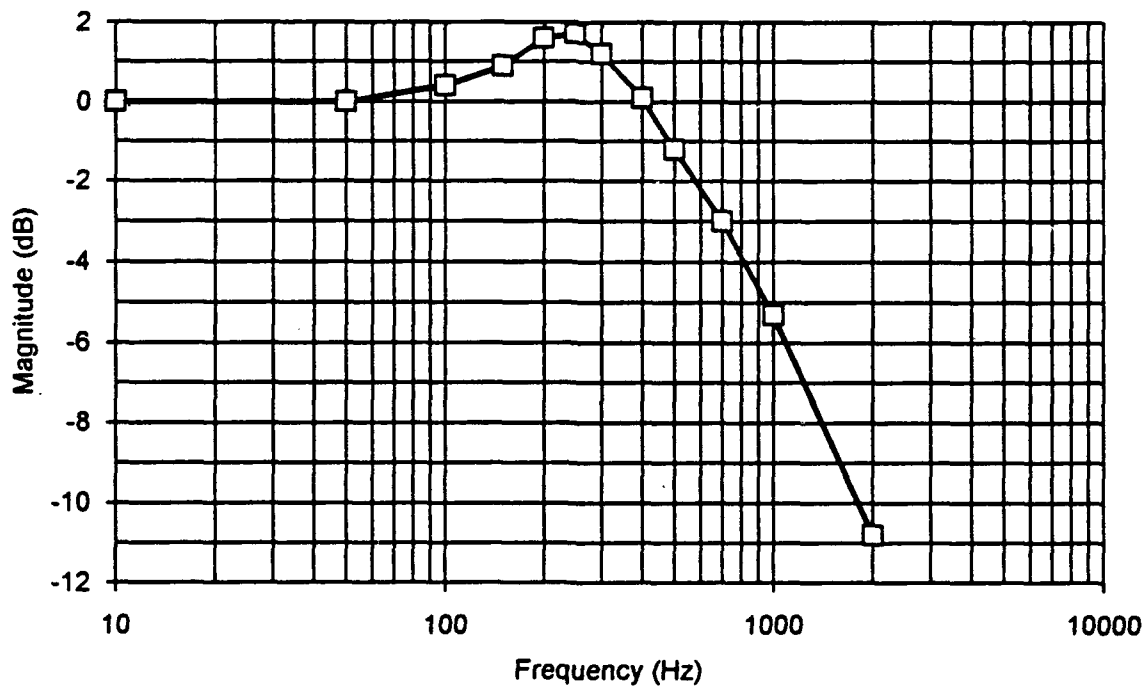


Figure 3.3.2.3-7 Closed Loop Response for the Carrier Loop at 32, 64, and 128 kbps

Figure 3.3.2.3-8 shows the frequency response for the 16 kbps data rate. This response should be the same as that obtained for the 32, 64, and 128 kbps data rates. However, a comparison of Figures 3.3.2.3-7 and 3.3.2.3-8 shows that there are slight differences in loop bandwidth and peaking for these two sets of data rates. These differences are caused by changes in the loop transport delay, which occur as the loop processing rate changes with data rate.

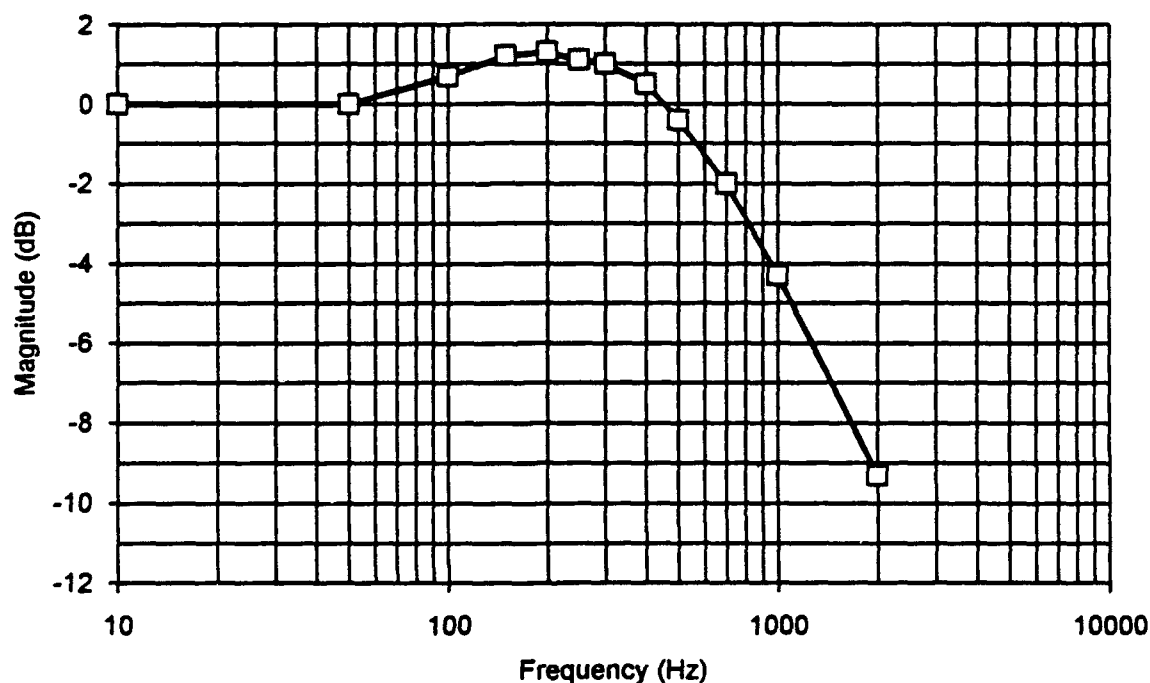


Figure 3.3.2.3-8 Closed Loop Response for the Carrier Loop at 16 kbps

The transport delay around the loop is approximately four times the processing rate period. The processing rate varies with data rate and can be obtained by dividing the accumulator rate, given in Table 3.3.2.3-1, by four. This results in a processing rate that is double the data rate for 32, 64, 128, 256, and 512 kbps and 32 times the data rate for 4, 8, and 16 kbps. By keeping the processing rate high, instability problems due to transport delay are eliminated.

The narrowest closed loop response occurs when operating at data rates of 4 and 8 kbps. The loop response, given in Figure 3.3.2.3-9, was measured at the 4 kbps data rate. In this case, the 3 dB bandwidth is 400 Hz and peaking is less than 2 dB.

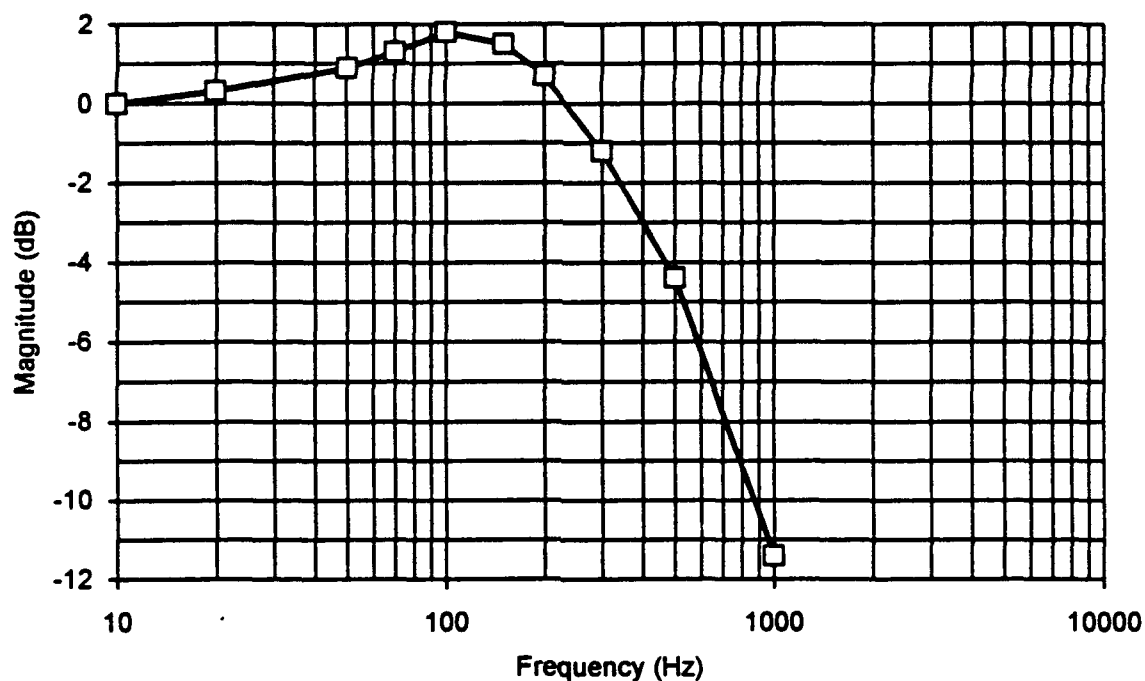


Figure 3.3.2.3-9 Closed Loop Response for the Carrier Loop at 4 and 8 kbps

The frequency acquisition range for the carrier tracking loop was measured for each data rate using an E_b/N_0 of 6 dB and a signal level of 1.5 volts peak-to-peak. The results, given in Table 3.3.2.3-3, show that acquisition range increases with data rate due to the increased closed loop bandwidth. The results also show that the carrier tracking loop meets the required ± 240 Hz acquisition range for all data rates.

Data Rate (kbps)	Frequency Acquisition Range
4	± 400 Hz
8	± 400 Hz
16	± 1.7 kHz
32	± 1.7 kHz
64	± 1.7 kHz
128	± 1.7 kHz
256	± 3 kHz
512	± 3 kHz

Table 3.3.2.3-3 Frequency Acquisition Range Versus Data Rate

The carrier tracking loop acquisition times were measured by applying a modulated signal as a step input and observing the transient response at the control input to the NCO. For these measurements, the time from leading edge of the step input until the transient response decayed to 1% of its final steady-state value was defined as the acquisition time of the carrier loop. The measurements were taken with a 200 Hz frequency offset between the carrier and the demodulator under noise free conditions and at an E_b/N_o of 6 dB. In both cases, the input signal level was 1.5 volts peak-to-peak.

Acquisition time was measured at three data rates (4, 64, and 512 kbps) to determine the response time of the loop at each of the bandwidths used by the demodulator. The results, given in Table 3.3.2.3-4, show that acquisition time improves with increased SNR and in all cases is well within the limits specified in Table 3.3-1.

Data Rate (kbps)	No Noise Condition	$E_b/N_o = 6$ dB Condition
4	4 ms	7 ms
64	600 μs	1.5 ms
512	200 μs	400 μs

Table 3.3.2.3-4 Acquisition Times for the Carrier Tracking Loop

3.3.2.4 Bit Synchronizer

When operating in coherent BPSK or non-coherent DPSK mode, a bit sync network is needed to synchronize the local clock with the receive data stream. Key performance requirements for the bit sync network are as follows:

- Fast clock sync acquisition
- Low RMS clock phase jitter when tracking the receive signal
- Capable of operating over a wide range of data rates (4 to 512 kbps)

A block diagram of the digital bit sync network is given in Figure 3.3.2.4-1. The design includes a dual bandwidth loop filter, to provide a wide bandwidth for rapid acquisition and a narrow bandwidth for low RMS phase jitter in track mode.

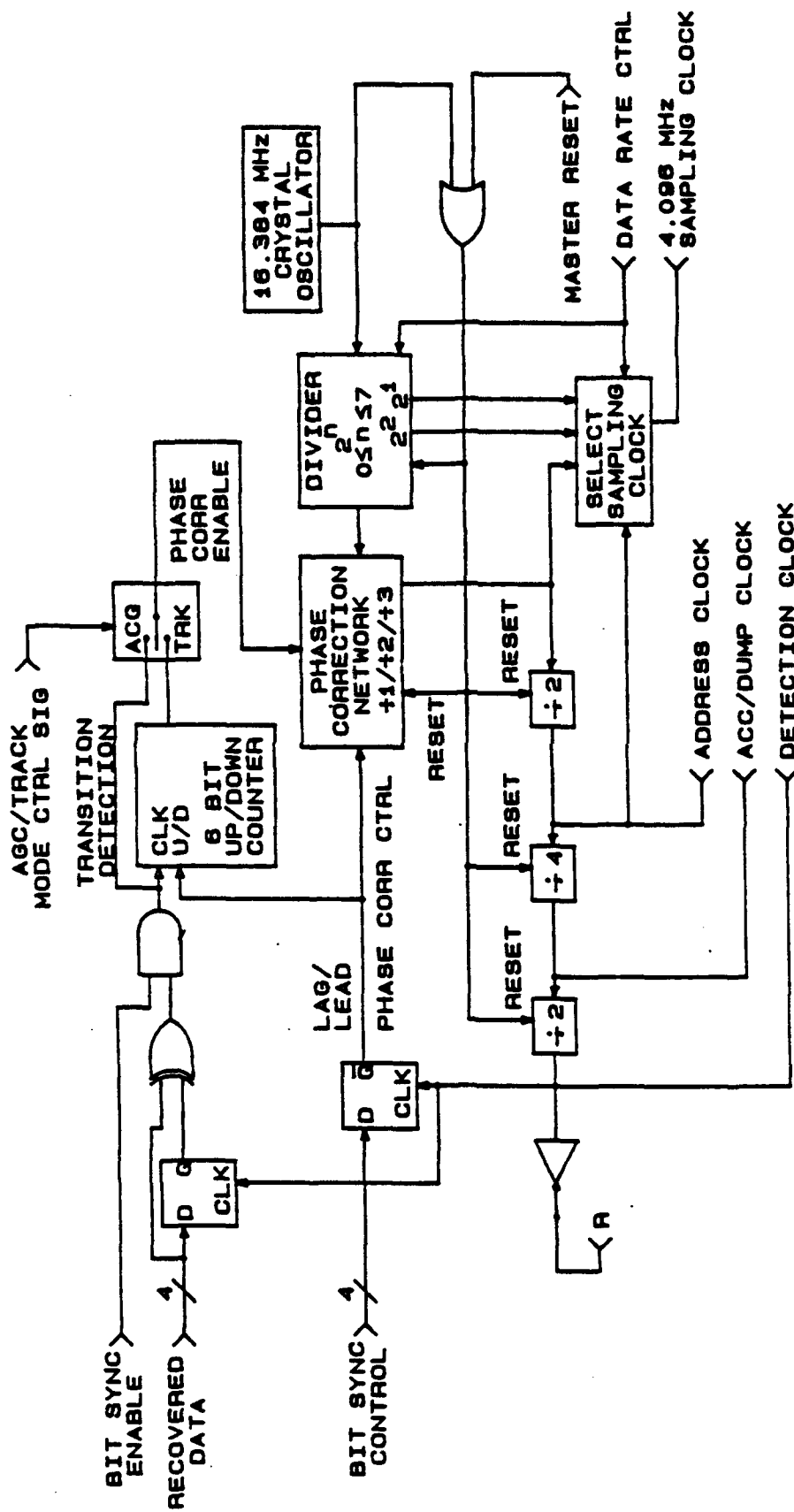


Figure 3.3.2.4-1 Bit Sync Network Block Diagram

During acquisition, a 6-bit Up/Down counter, which acts as the digital loop filter, is bypassed and lag/lead decisions are sent directly to the loop phase correction network. In this mode, phase corrections are made each time a bit transition is detected. The size of the phase correction is 11.25 degrees and the direction of the phase correction is controlled by the lag/lead signal. When tracking the received signal, the bit sync loop must provide low RMS phase jitter. This is achieved by switching in the 6-bit Up/Down counter which averages the number of lag/lead decisions before making a phase correction.

Measured Test Results

The following parameters were measured on the bit synchronizer to verify that it meets the performance requirements specified in Table 3.3-1:

- Frequency Acquisition Range
- Acquisition Time
- Bit Error Rate Performance

The frequency acquisition range of the bit sync loop was measured by applying a DPSK modulated signal source to the modem and adjusting the frequency of the data rate clock at the transmit signal source until the bit sync loop could no longer acquire sync. Tests were conducted in both acquisition and track mode while operating at data rates of 4, 64, and 512 kbps. All measurements were taken under noise free conditions.

The results of the test, given in Table 3.3.2.4-1, show that the acquisition and track bandwidths differ by a factor of 32:1. The results also show that the bit sync loop can tolerate frequency errors of greater than 500 PPM when operating in both acquisition and track mode, which is well within the frequency accuracy of the data rate clock.

Data Rate (kbps)	Acquisition Range	Track Range
4	+64.5 Hz -63.5 Hz	+2 Hz -3.9 Hz
64	+1.03 kHz -660 Hz	+32 Hz -63 Hz
512	+8.26 kHz -6.4 kHz	+262 Hz -500 Hz

Table 3.3.2.4-1 Bit Sync Frequency Acquisition Range

The bit synchronizer acquisition times were measured at E_b/N_0 ratios of 4, 6, and 8 dB. The tests were conducted with the demodulator in noncoherent DPSK mode to eliminate any effects that could be introduced by the carrier tracking loop. The results given in Table 3.3.2.4-2, show that when operating at an E_b/N_0 of 6 dB or greater, the bit sync network meets the acquisition time requirements specified in Table 3.3-1.

Data Rate (kbps)	Acquisition Time		
	$E_b/N_0 = 4$ dB	$E_b/N_0 = 6$ dB	$E_b/N_0 = 8$ dB
4	< 17 ms	< 14.5 ms	< 11 ms
8	< 8.5 ms	< 6.0 ms	< 4.2 ms
16	< 4.2 ms	< 2.5 ms	< 1.5 ms
32	< 2.5 ms	< 1 ms	< 750 μ s
64	< 1.2 ms	< 750 μ s	< 550 μ s
128	< 750 μ s	< 600 μ s	< 450 μ s
256	< 350 μ s	< 200 μ s	< 120 μ s
512	< 150 μ s	< 120 μ s	< 90 μ s

Table 3.3.2.4-2 Bit Sync Acquisition Times In Noncoherent DPSK Mode

When operating in BPSK mode, the carrier tracking loop and bit synchronizer acquire sync at the same time. Table 3.3.2.4-3 shows the worst case acquisition times for BPSK mode at an E_b/N_0 ratio of 6 dB.

Data Rate (kbps)	Acquisition Time
4	19.5 ms
8	10 ms
16	4 ms
32	2.5 ms
64	2 ms
128	1.4 ms
256	600 μ s
512	520 μ s

Table 3.3.2.4-2 Worst Case Bit Sync Acquisition Times In BPSK Mode

The bit-error-rate (BER) performance of the demodulator was measured for coherent and noncoherent operation at data rates of 4, 64, and 512 kbps. The results, given in Figures 3.3.2.4-2 thru 3.3.2.4-7, show that the demodulator implementation losses are less than 1.5 dB under all the conditions.

It should be noted that these tests were conducted before the demodulator was installed in the brassboard modem and integrated with the RF section. As a result, the predetection filter bandwidths used for these tests are slightly different than those used in the final design. There could be slight differences between the BER performance indicated in the figures and that of the final design. However, the information given in this report is the most accurate data available at this time.

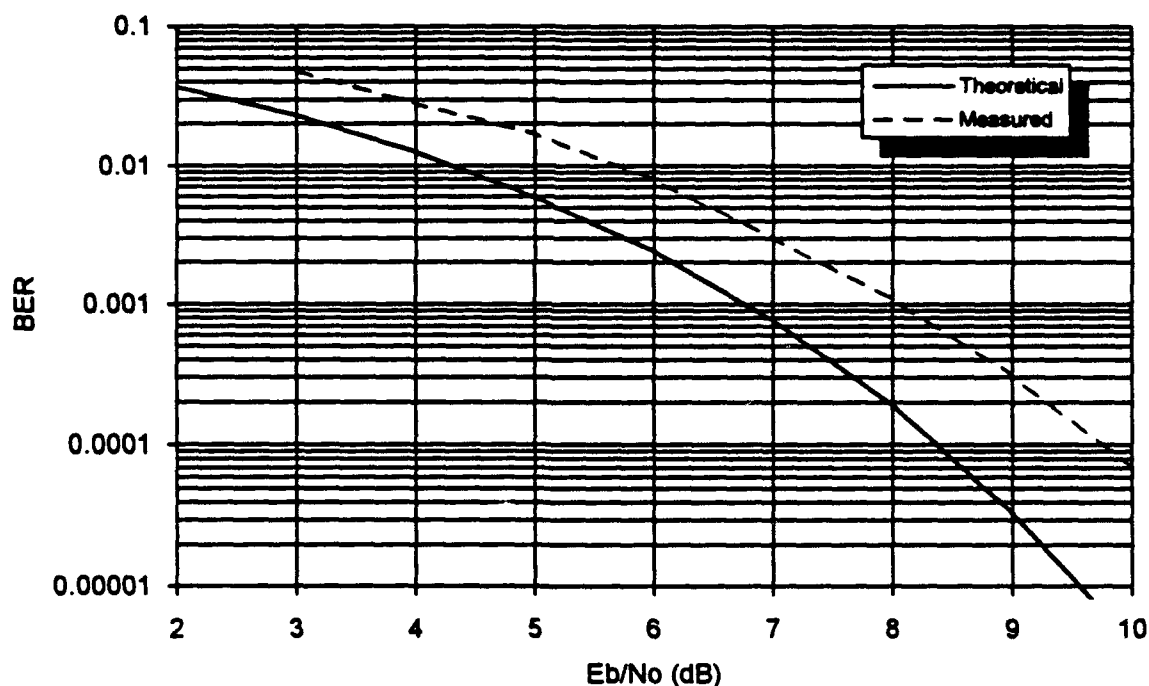


Figure 3.3.2.4-2 BPSK Demod Performance at 4 kbps Measured
With a Predetection Bandwidth of 16 kHz

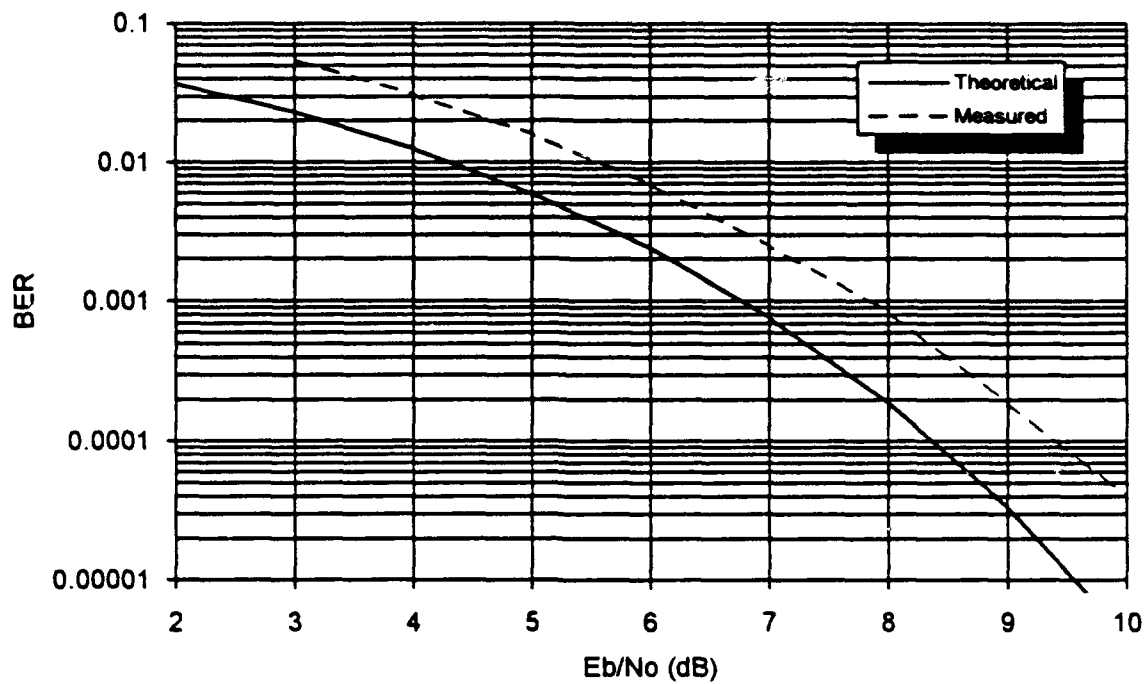


Figure 3.3.2.4-3 BPSK Demod Performance at 64 kbps Measured
With a Predetection Bandwidth of 250 kHz

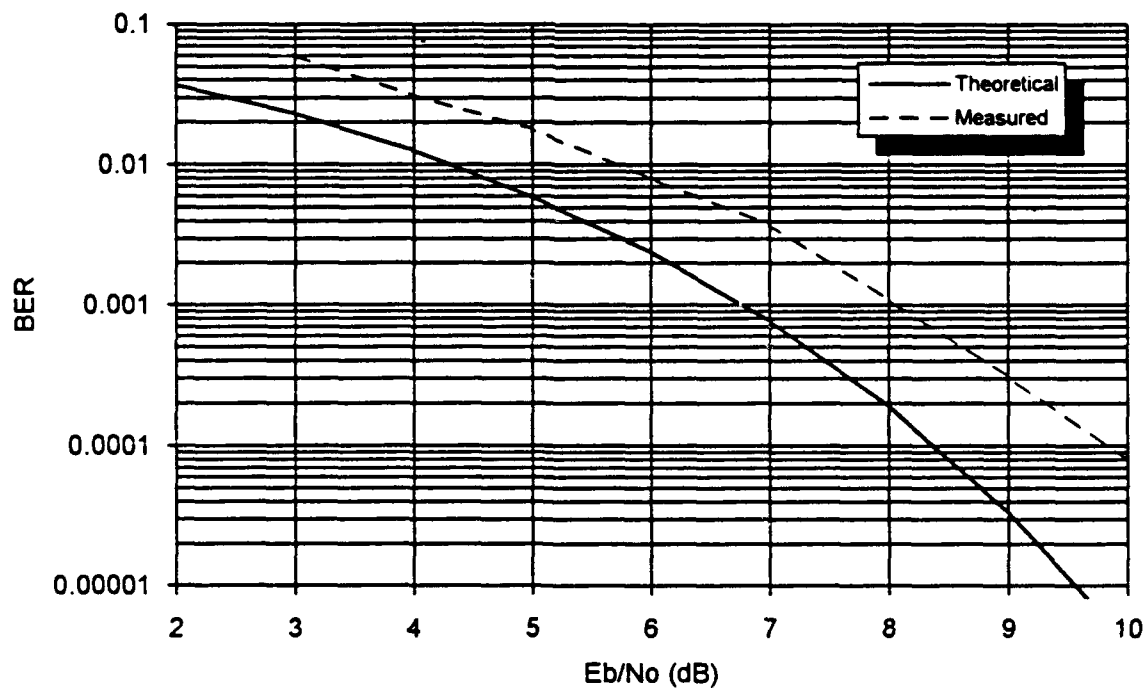


Figure 3.3.2.4-4 BPSK Demod Performance at 512 kbps Measured
With a Predetection Bandwidth of 1 MHz

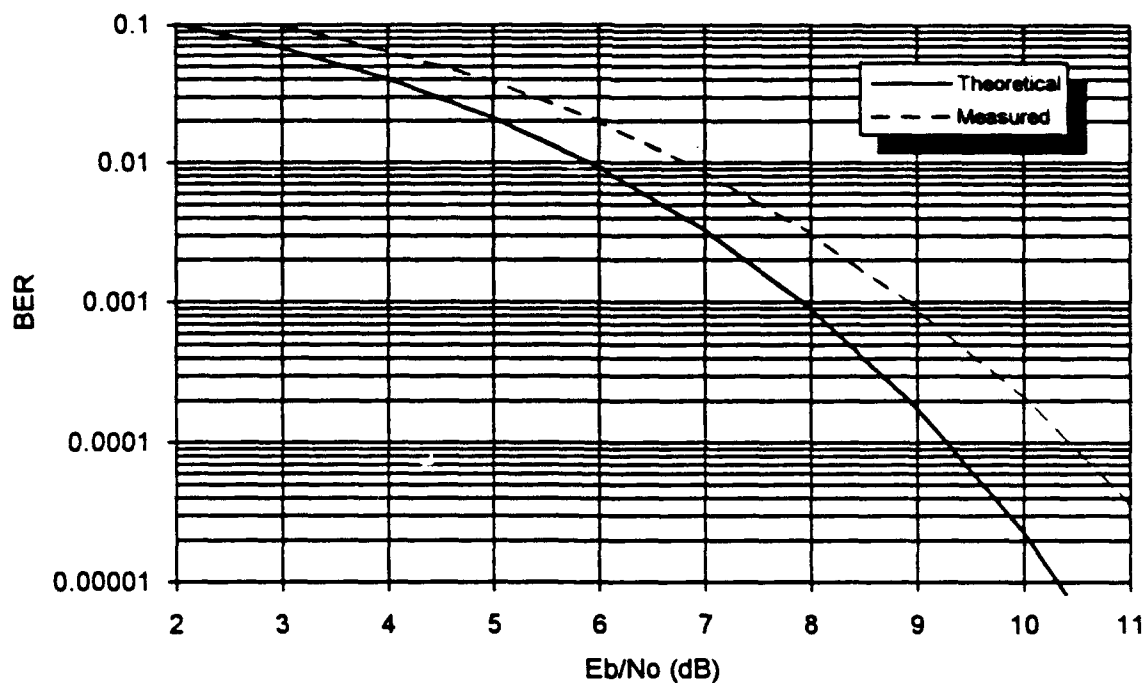


Figure 3.3.2.4-5 DPSK Demod Performance at 4 kbps Measured
With a Predetection Bandwidth of 16 kHz

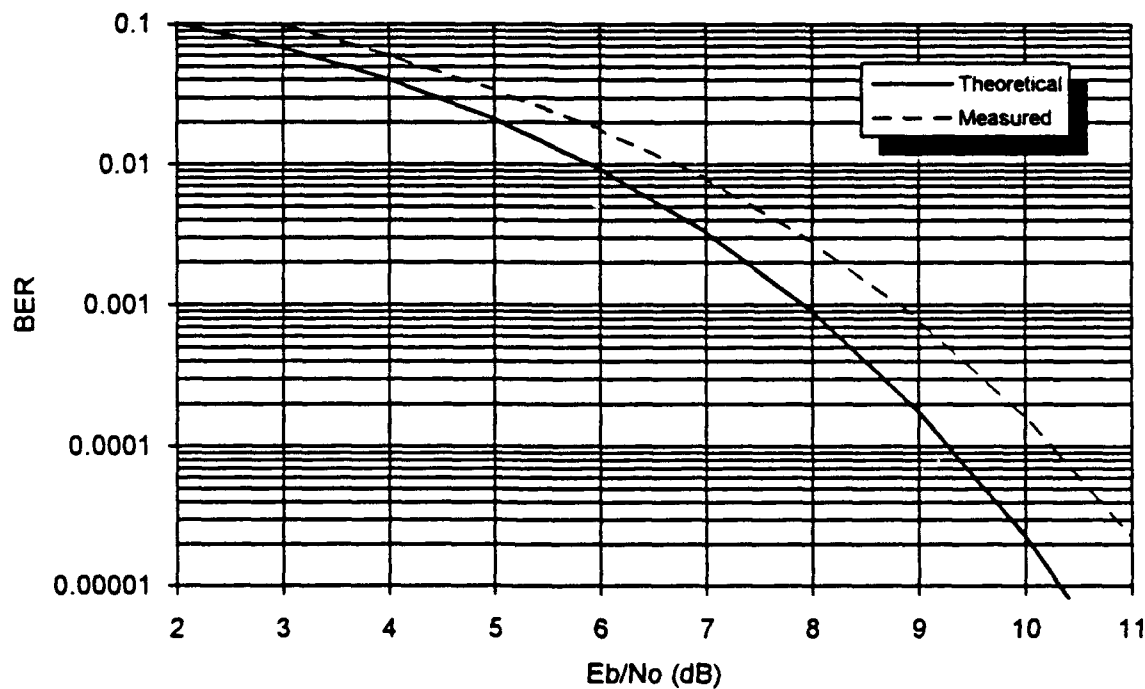


Figure 3.3.2.4-6 DPSK Demod Performance at 64 kbps Measured
With a Predetection Bandwidth of 250 kHz

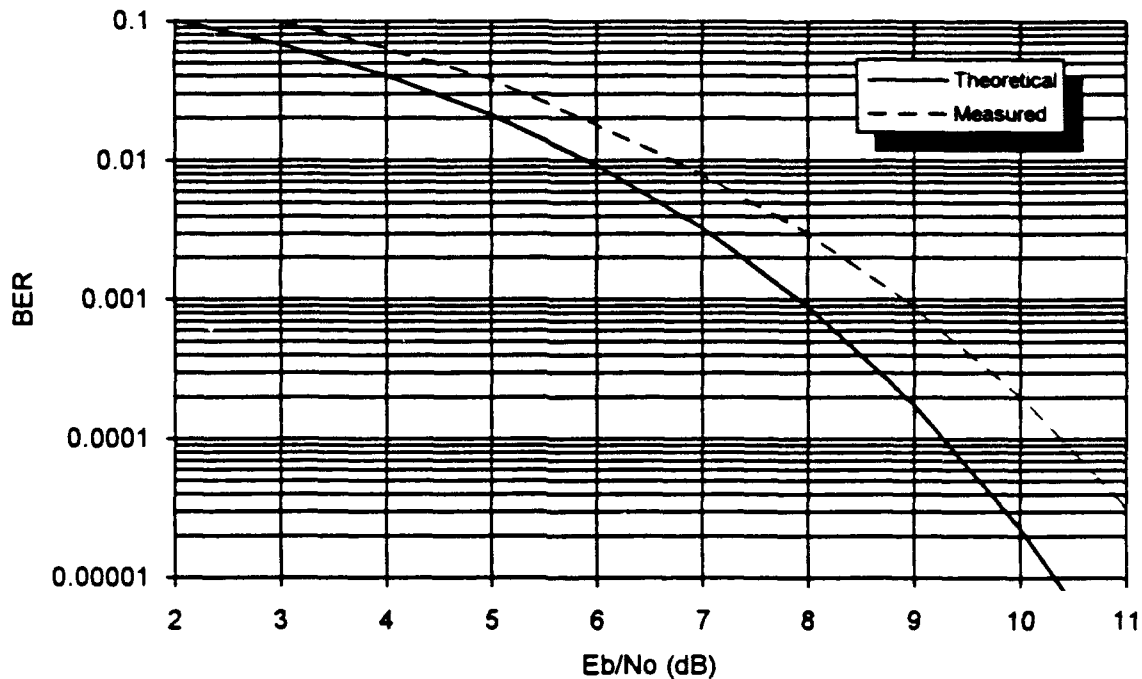


Figure 3.3.2.4-7 DPSK Demod Performance at 512 kbps Measured
With a Predetection Bandwidth of 1 MHz

3.3.2.5 Sync and M-ary Symbol Detection

The sync correlator and M-ary symbol detection circuit block diagram is shown in Figure 3.3.2.5-1. Although the M-ary symbol detection portion of the circuit isn't used in the final design, the hardware is shown on the block diagram because still exists in the modem. This primary functional requirements of the circuit are as follows:

- Binary sync detection
- M-ary sync detection
- M-ary symbol decode

Initialization and control of the sync detect circuit is provided by a state machine. During initialization, the state machine resets the correlators, the sync accumulators, and the data buffers, and loads the correlators with the required reference code. Once the correlators have been loaded and all circuitry has been reset, binary sync detection can begin.

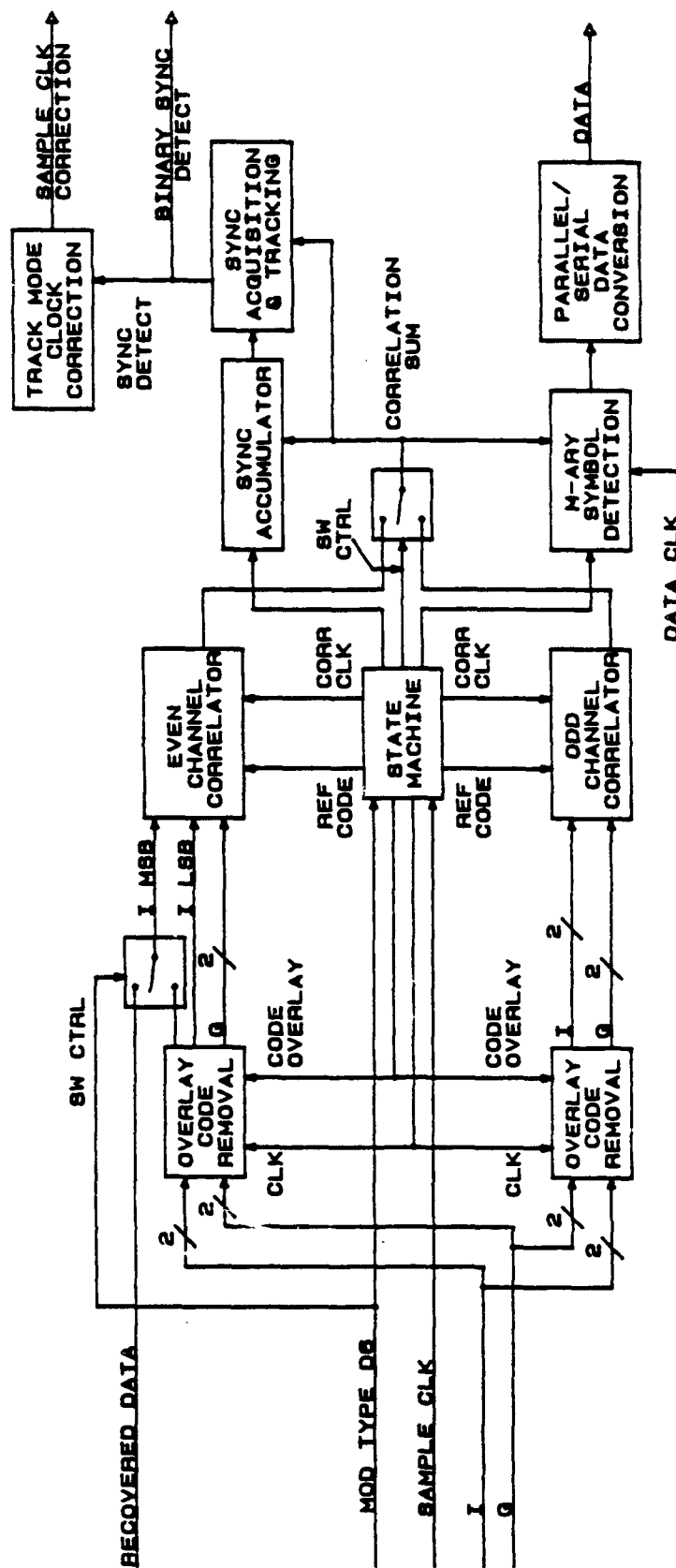


Figure 3.3.2.5-1 Sync and M-ary Symbol Detection Block Diagram

In binary mode, recovered baseband data from the BPSK/DPSK demodulator is applied to the most-significant-bit (MSB) of the even channel correlator for comparison with a 32-bit reference code. Binary sync detection is declared when the number of bit agreements between the incoming data stream and the 32-bit reference code exceeds a specified threshold. The threshold is adjustable using DIP switches located on the correlator board in the demodulator section of the modem.

A description of how the circuit would operate in M-ary mode, is given in the Design Plan and will not be repeated here since it isn't used in the present design.

3.4 RF/IF Section

The RF/IF section of the modem consists of six modules; an RF preamplifier, tuner, IF module, transmit synthesizer, receive synthesizer, and transmit modulator. The RF preamplifier is a broadband RF amplifier supplied by Qbit Corporation. The tuner and synthesizer modules are existing designs presently used in the AN/PRC-119 (SINCGARS) manpack radio. The IF module and transmit modulator are newly developed items for this program.

The overall receiver RF/IF architecture is shown in Figure 3.4-1 along with performance budgets for gain, noise figure (NF), and image rejection. Incoming signals within the 40 to 60 MHz frequency range are selectively amplified by the RF preamp and tuner modules and then downconverted to a first IF of 10.7 MHz. Electronically tunable, 2-pole, bandpass filters in the tuner module provide a total of 85 dB image rejection (@ $f = LO + 10.7 \text{ MHz}$) prior to the first mixer. The 10.7 MHz output signal from the tuner module is amplified and filtered in the IF module and then downconverted to a 7.5 MHz second IF. The second IF is downconverted to baseband In-Phase (I) and Quadrature (Q) channels, which are output to the digital demodulator. Automatic gain control (AGC) is included in the IF module to provide a constant baseband output level for all RF input signal levels from -123 to -83 dBm.

3.4.1 RF Preamplifier

The RF preamplifier consists of a pair of cascaded highpass/lowpass filters followed by a broadband, low noise, RF amplifier. Theoretically, an RF preamplifier isn't needed to meet the gain or NF requirements of the receiver. However, in cases such as this where a sensitive receiver and high digital logic circuits are located in close proximity, harmonics of the high speed clocks often couple into the front-end of the receiver and degrade sensitivity on some discrete frequencies. This is especially true at the lower data rates where sensitivity is less than -120 dBm. A well shielded RF preamplifier, located directly at the receiver RF input, solves this problem by boosting the receive signal level before it becomes contaminated with noise.

The preamplifier selected for the modem design has 15 dB of gain and a NF of 3 dB. The cascaded highpass/lowpass filters, which precede the RF amplifier, attenuate signals outside the desired operating band of 40 to 60 MHz. A high input compression level



Figure 3.4-1 Receiver RF/IF Architecture

(+6 dBm) minimizes the possibility that large in-band signals can overdrive the RF preamplifier and degrade receiver sensitivity.

3.4.2 Tuner

The tuner module accepts receive signals from the low noise RF preamp and downconverts them to a 10.7 MHz IF by mixing with a local oscillator (LO) signal from the receive synthesizer. A block diagram of the tuner module is given in Figure 3.4.2-1. The tuner consists of an input 2-pole filter, followed by a single stage RF amplifier, an output 2-pole filter, and a passive double balanced mixer. The 2-pole, binary tuned, filters use PIN diodes to switch binary weighted capacitors for tuning. The filters are capable of tuning from 30 to 88 MHz, however, only the 40 to 60 MHz range is used for this application. The desired center frequency is selected through frequency control information supplied by the modem controller.

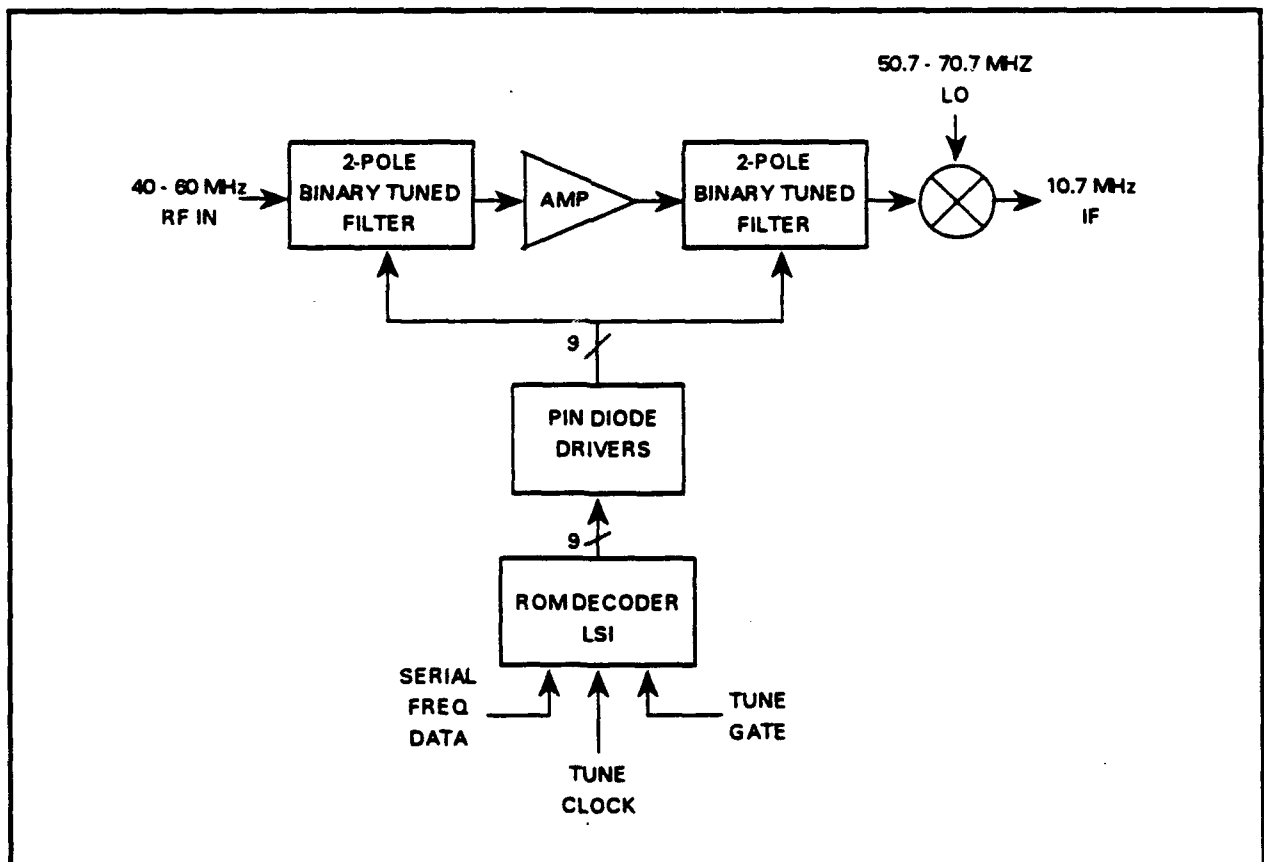


Figure 3.4.2-1 Tuner Block Diagram

Tuner performance specifications are given in Table 3.4.2-1. The 1 dB bandwidth is a minimum of 1 MHz over the frequency range from 40 to 60 MHz, which is sufficient to pass BPSK modulated signals with data rates up to 512 kbps. A maximum NF of 6.5 dB and a minimum gain of 4 dB ensures that the overall receive NF is less than 6 dB.

Item	Specification
Frequency Range (fo)	40 to 60 MHz
Gain	4 dB Min, 7 dB Max
Image Rejection	80 dB Min (fo + 21.4 MHz)
IF Rejection	100 dB Min
LO Radiation	-73 dBm @ RF Input Port
Noise Figure	6.5 dB
1 dB Compression Level	-5 dBm @ Tuner RF Input
3rd Order Intercept Point	+6 dBm
Selectivity: fo ± 500 kHz fo ± 1.5 MHz fo ± 10 MHz	1 dB Max 8 dB Min 48 dB Min
Input VSWR (50-Ohm System)	2.5:1
Output VSWR (50-Ohm System)	2.5:1

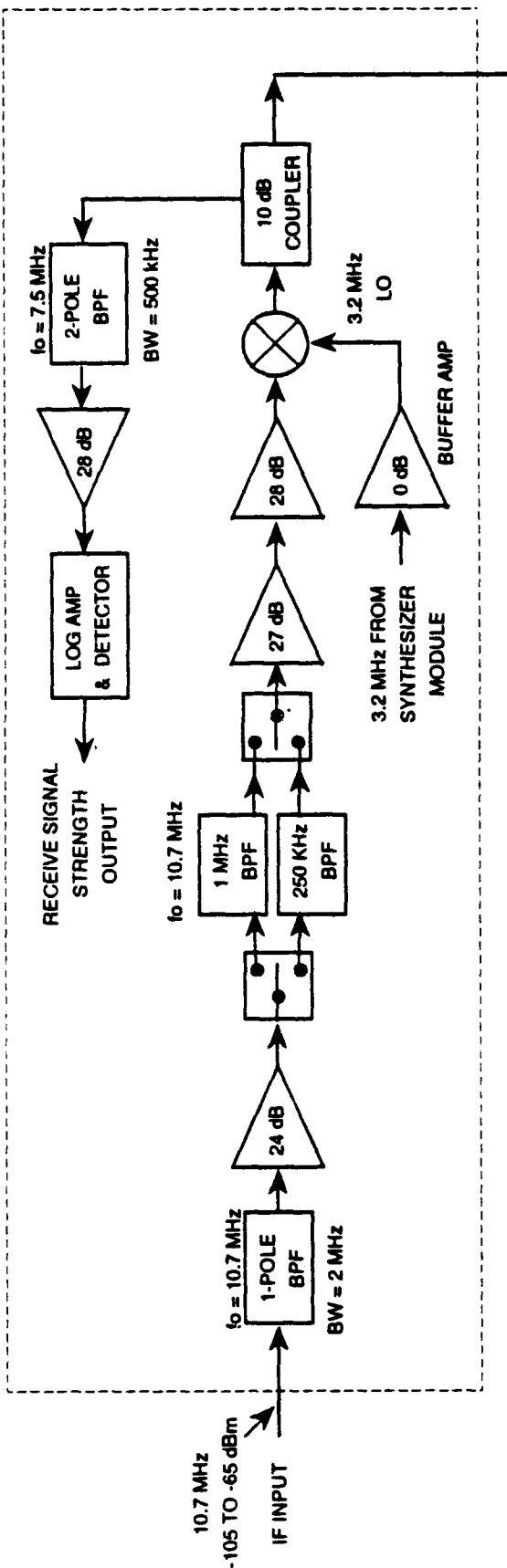
Table 3.4.2-1 Tuner Performance Specifications

3.4.3 IF Module

The IF module accepts low level receive IF signals from the tuner module and performs the analog signal processing required before the signal can be digitized. As shown in Figure 3.4.3-1, the 10.7 MHz IF input is amplified, bandpass filtered (BPF), and then mixed with a 3.2 MHz LO for downconversion to the 7.5 MHz second IF frequency. A dual conversion, IF architecture was selected to minimize the amount of gain required at any one IF frequency and reduce the risk of undesired oscillations due to undesired coupling between the input and output stages. This in turn simplifies the layout and shielding requirements placed on the IF module.

Switchable bandpass filters are included in the 10.7 MHz signal path to control the noise bandwidth of IF at the higher data rates and to filter off undesired mixing products. The 7.5 MHz second IF is split into two paths and applied to quadrature mixers to produce

BOARD NO 1



BOARD NO 2

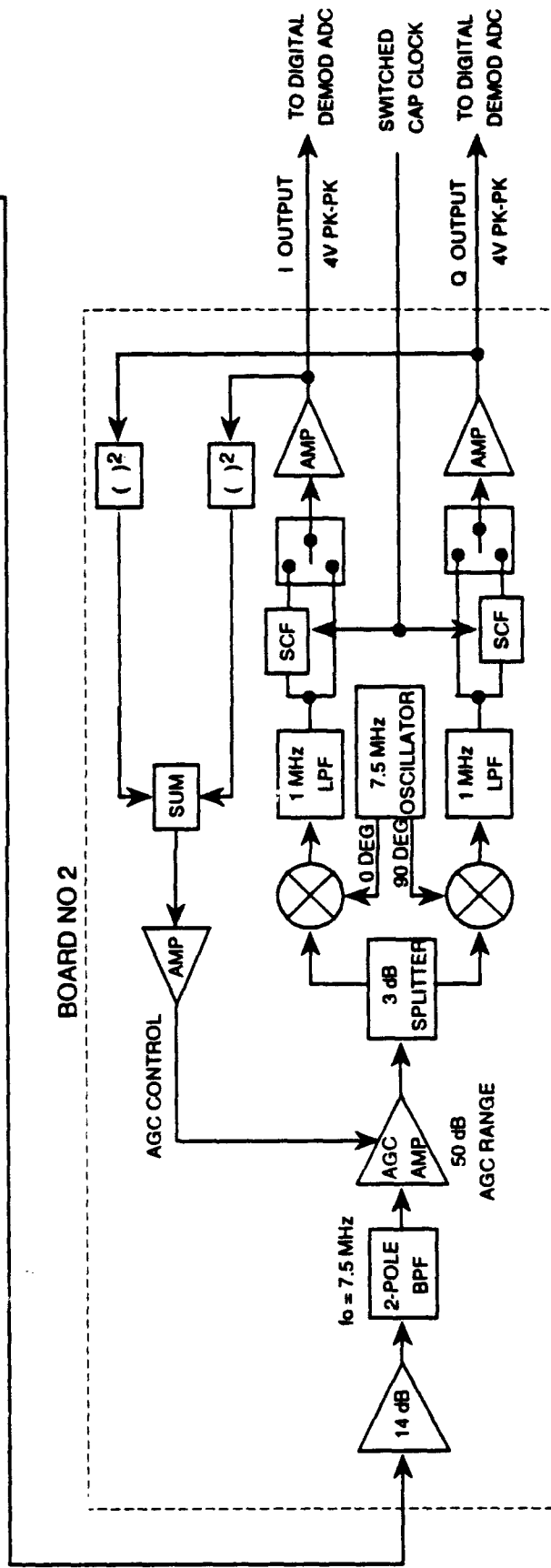


Figure 3.4.3-1 IF Block Diagram

the baseband I and Q signal components. The I and Q channels are then amplified and applied to switched capacitor lowpass filters, which have a tunable cutoff frequency that is controlled through the use of a variable frequency clock. At data rates of 128 kbps or greater, the baseband signals are routed around the switched capacitor filters (SCF) because the signal bandwidth exceeds the 95 kHz maximum cutoff frequency of the SCF. The bandwidth and filter combinations used for each data rate are defined in section 3.3.2.1.

Automatic gain control (AGC) is derived from the I and Q baseband outputs. The AGC circuit is adjusted to provide a maximum output level of 4.4 V Pk-to-Pk going into the analog-to-digital converters (ADC) in the digital demodulator.

3.4.4 Synthesizer

Standard SINCGARS synthesizer modules are used to generate local oscillator (LO) frequencies for the receiver first IF mixer and the transmit modulator. The receive synthesizer also provides a 3.2 MHz signal to the IF module that is used as the LO for the receiver second IF mixer. The synthesizer performance specifications are summarized in Table 3.4.4-1.

A block diagram of the synthesizer module is given in Figure 3.4.4-1. The synthesizer design is centered around a single voltage tuner oscillator (VTO) that is phase locked to a 3.2 MHz frequency standard. The 3.2 MHz source is a temperature compensated crystal oscillator (TCXO) that has a frequency accuracy of ± 1 PPM at room temperature. The VTO's frequency is controlled by a programmable digital counter and is capable of tuning from 37 to 100.475 MHz in five bands. Only the 40 to 70.7 MHz frequency range is used for this application. A serial tuning word supplied by the modem controlled is used to select the desired VTO band and set the programmable counter in the feedback path to the phase detector.

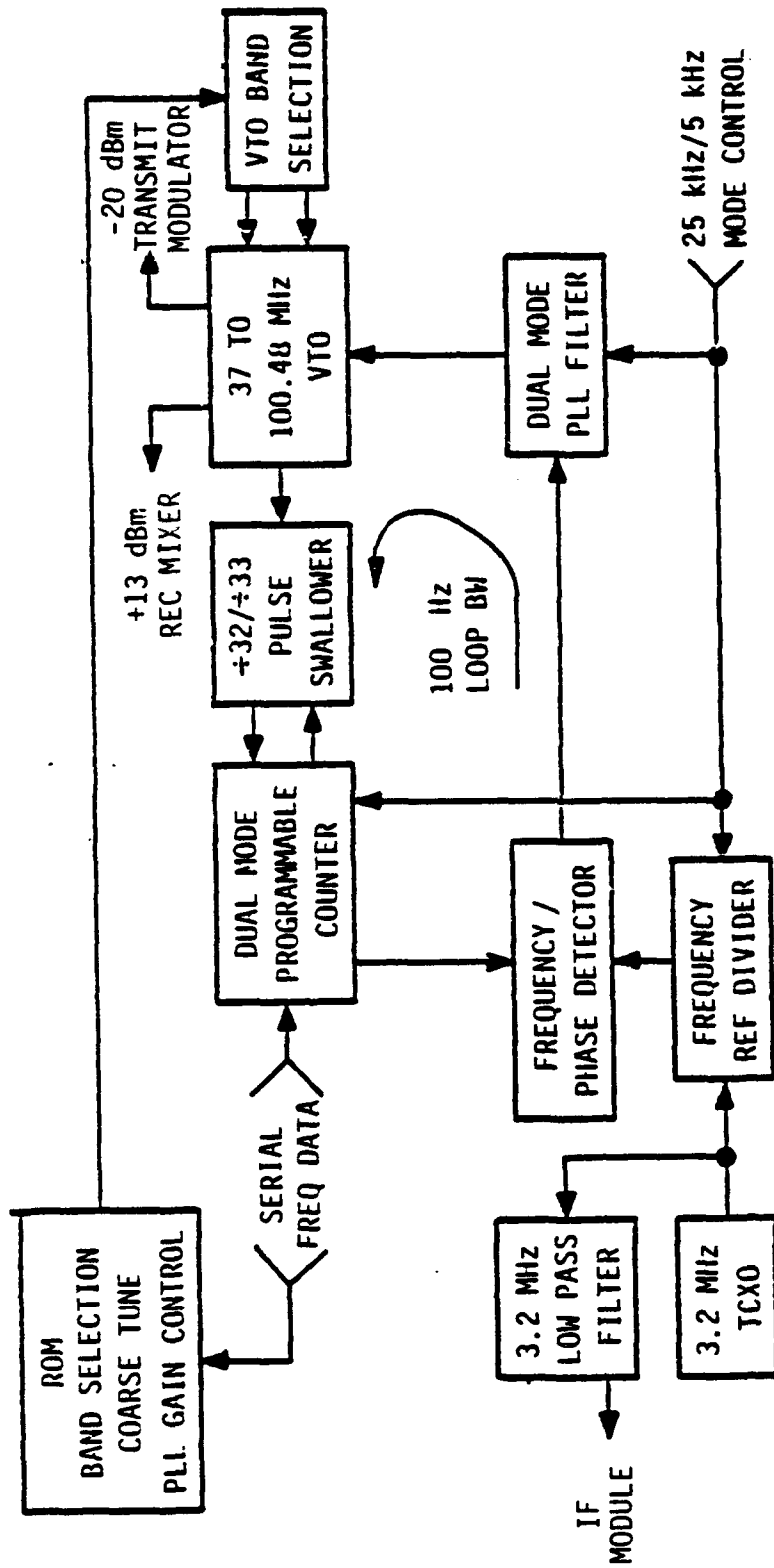


Figure 3.4.4-1 Synthesizer Block Diagram

Item	Specification
LO Output:	
Frequency	40.000 to 70.700 MHz
Tuning Resolution	25 kHz
Frequency Accuracy	± 1 PPM
Output Level	+ 13 dBm
Harmonics	-30 dBc max
Spurious	< -55 dBc
TCXO Reference Output:	
Frequency	3.2 MHz ± 1 PPM
Output Level	Sinusoid, 0 to 5V Peak-Peak

Table 3.4.4-1 Synthesizer Performance Specifications

3.4.5 Transmit Modulator

The transmit modulator accepts an unmodulated RF carrier from the transmit synthesizer and generates a biphase modulated carrier. As shown in the block diagram of Figure 3.4.5-1, transmit baseband data is amplified and applied to the IF port of a passive double balanced mixer. The polarity of the RF carrier out of the mixer is inverted or non-inverted based on the polarity of the baseband data applied to the dc-coupled IF port. The BPSK modulated output from the mixer is amplified to +22 dBm and then low pass filtered to attenuate transmitter harmonics to less than -50 dBc.

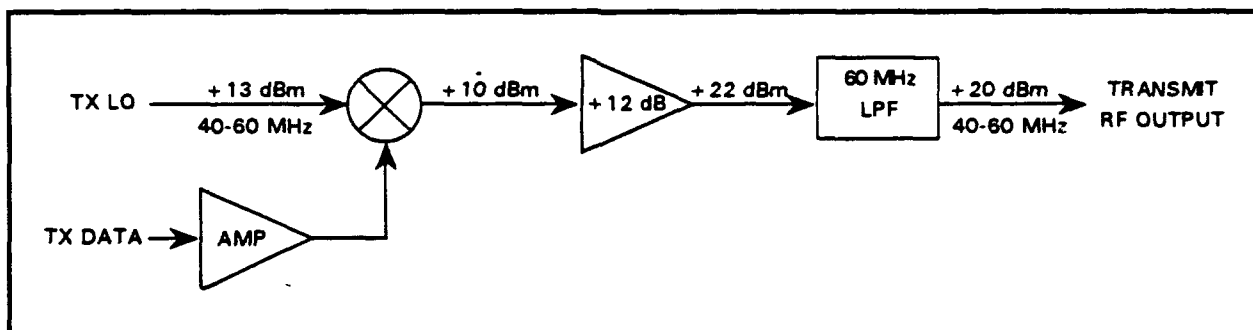


Figure 3.4.5-1 Transmit Modulator Block Diagram

SECTION 4

SYSTEM SOFTWARE DESIGN

The system consists of two computer controlled devices, the control terminal and modem controller. This section of the Final Report briefly describes the software programs that were developed for both of these devices.

4.1 Control Terminal

The control terminal's software program allows the meteor burst operator to set up the modem controller and process both transmit and receive messages. The control terminal software includes setup, diagnostic, message management, and control routines. This program runs on an ITT XTRA/386 PC, which connects to the modem controller through the RS-232 serial communications port.

The control terminal software is written in the programming language C and is compiled for the ITT XTRA/386 PC using Microsoft's version 5.0 C compiler.

4.1.1 Control Terminal Software Requirements

The control terminal software requirements are as follows:

- The control terminal software shall allow the operator to prepare, edit, delete, or select a transmit message.
- The control terminal software shall allow the control terminal operator to select the transmit and receive data rates (4 kbps, 8 kbps, 16 kbps, 32 kbps, 64 kbps, 128 kbps, 256 kbps, 512 kbps).
- The control terminal software shall allow the control terminal operator to select either BPSK or DPSK modulation format.
- The control terminal software shall allow the control terminal operator to set the time and date.
- The control terminal software shall send a message selected by the control terminal operator to the modem controller via the RS-232 communications link.

- The control terminal software shall display acknowledgments to transmitted message packets.
- The control terminal software shall enable or disable the modem transmitter.
- The control terminal software shall print the database information
- The control terminal software shall receive, display, and store messages from the modem controller.

4.1.2 Control Terminal Software Functions

Upon initial power-up, the control terminal software performs the tasks necessary to initialize the control terminal and the modem controller. During normal operation, the control terminal software interfaces with the modem controller, printer and disk drives and coordinates activities between the functional areas shown in the block diagram of Figure 4.1.2-1.

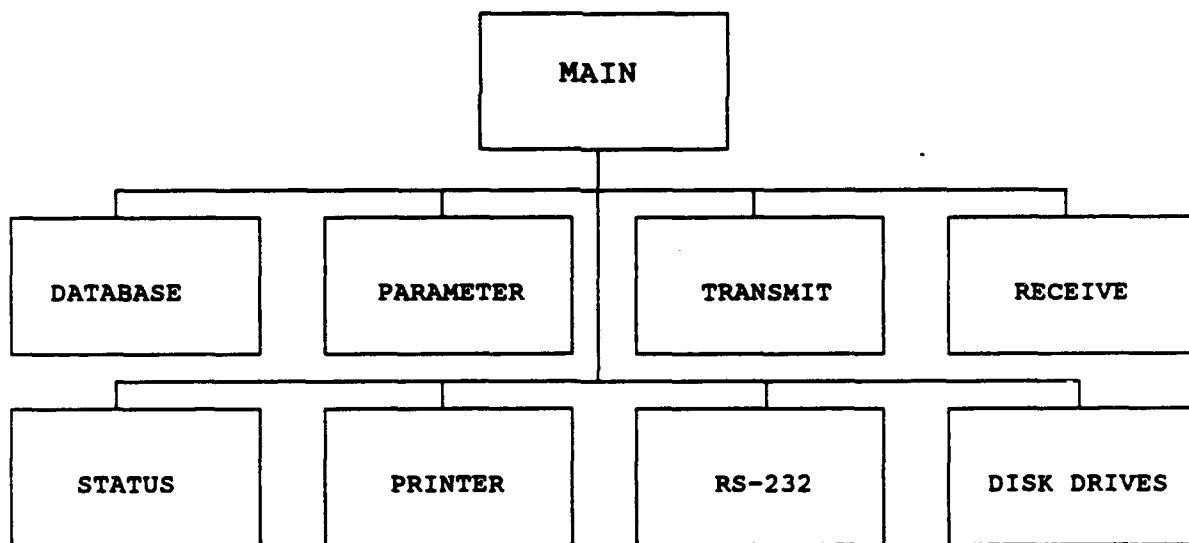


Figure 4.1.2-1 Control Terminal Software Functional Block Diagram

The DATABASE functions allow the operator to access the transmit message, receive message, meteor trail, and statistics databases. Functions available under the DATABASE routines are as follows; review, edit, delete one, print one, print all, or clear all any of the above databases.

The PARAMETER function is used to set up the different settings of the modem. The transmit frequency, receive frequency, data rate, modulation, source address, destination address, date, time, printer, coding are defined within this function.

The TRANSMIT and RECEIVE functions handle disk storage and retrieval. The TRANSMIT routines also allow the operator to select the message to be sent. The RECEIVE routines continually routine the RS-232 port for receive information from the modem controller. The TRANSMIT and RECEIVE functions also allows the operator to send commands to the modem.

The STATUS functions provide immediate feedback to the control terminal operator on message traffic. These routines display the status of the modem, messages received over the modem, and status of the message being sent over the modem.

The SYSTEM TEST functions are used to verify the operation of the modem; Self test, BER test transmit, BER test receive, Transmit test, transmit loopback, and BER loopback. The self test verifies the RAM, ROM, Reed-Solomon hardware, TX/RX baseband control hardware, and the RS-232 interface. Functions are provided to setup the modem for transmitting or receiving BER testing between modems. A function is provided to set the modem transmitting a continuous pattern for spectrum analysis. Transmit loopback function is provided so that the transmit and receive RF hardware of the modem can be tested without another modem. A BER loopback function is also provided for single modem analysis.

4.2 Modem Controller

The modem controller software program handles communications between the control terminal and the single board computer (SBC). This includes processing messages to be sent over the meteor burst link plus setting up the modem hardware so that it can send and receive these messages. The software sets up the modem's hardware, in accordance with the parameters supplied by the control terminal via the RS-232 communications link.

The modem communicates over a meteor burst link using the protocol defined in section 2.2. When communicating over a meteor burst link, the modem controller software processes receive data from the demodulator to determine when a link has been established and what should be done in response.

The modem controller program flow diagram is shown in Figure 4.2-1. Notice that the interface between the control terminal and the baseband hardware is handled by interrupts. This minimizes processing time and allows the modem controller to meet the stringent timing requirements placed upon the system by high data rates at which it must operate.

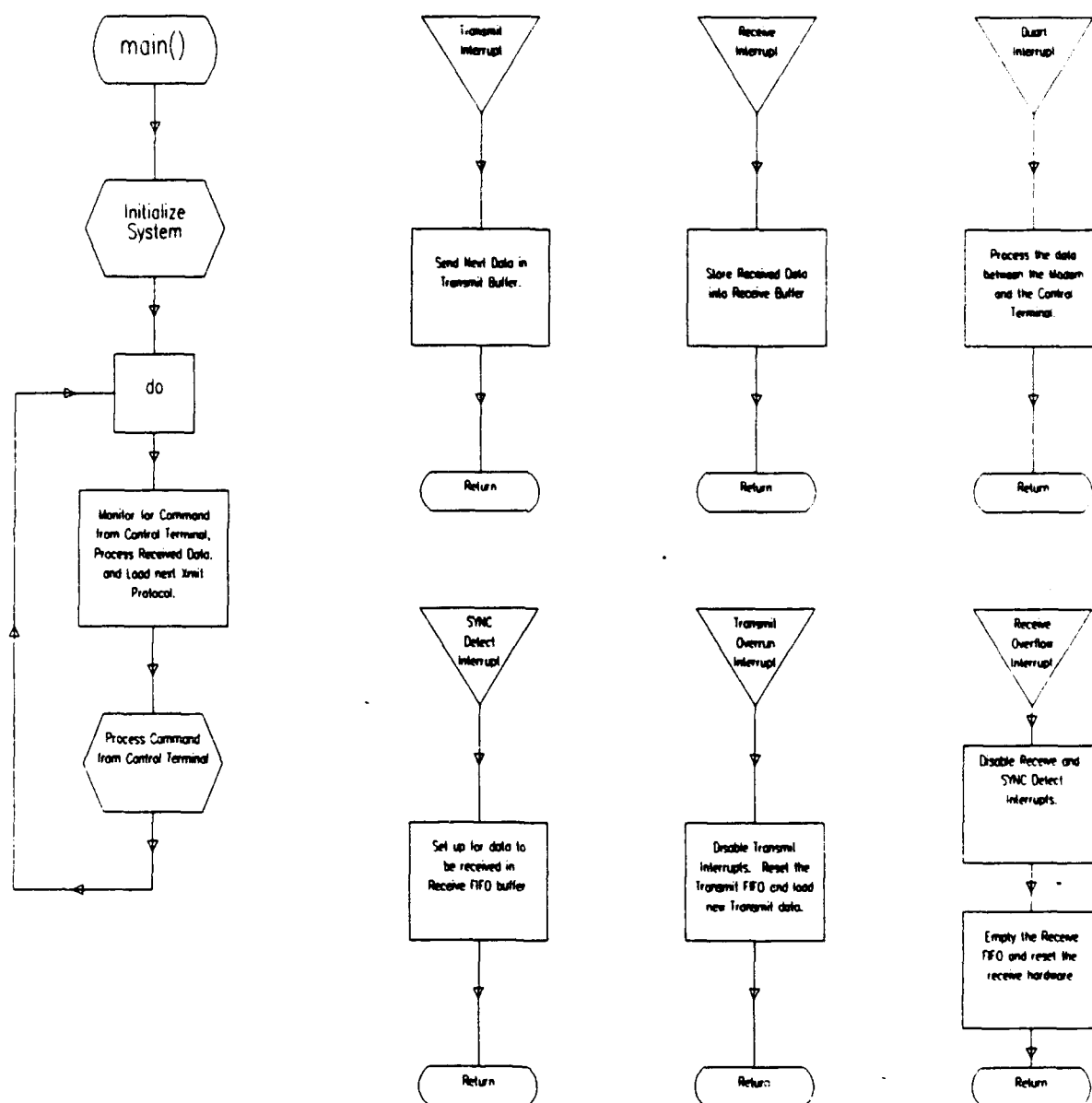


Figure 4.2-1 Modem Controller Program Flow Diagram

The program is written in the programming language C and is cross compiled with Microtek's C cross compiler for the Motorola 68020 microprocessor. The compiled program

is burned into four (4) 1 Mbyte x 8 EPROM's, which are installed on the single board computer (SBC).

4.2.1 Modem Controller Software Requirements

The modem controller software requirements are as follows:

- The modem controller software shall transmit and receive message traffic over a meteor burst link.
- The modem controller software shall implement the link protocol defined in section 2.2 of this report.
- The modem controller software shall enable or disable the transmit RF modulator.
- The modem controller software shall select the transmit message source as specified by the control terminal operator.
- The modem controller software shall set the transmit and receive data rates (4 kbps, 8 kbps, 16 kbps, 32 kbps, 64 kbps, 128 kbps, 256 kbps, & 512 kbps).
- The modem controller software shall set the modulation format specified by the control terminal operator (BPSK or DPSK).
- The modem controller software shall set the time and date supplied by the control terminal operator.
- The modem controller software shall set the transmit and receive operating frequencies as specified by the control terminal operator.
- The modem controller software shall tune the transmit synthesizer module.
- The modem controller software shall tune the receive synthesizer and tuner module.
- The modem controller software shall send formatted transmit messages to the baseband controller.
- The modem controller software shall receive acknowledgments to the transmitted messages.

- The modem controller software shall receive and store a received message from the baseband controller.
- The modem controller software shall transfer receive messages to the control terminal.
- The modem controller software shall monitor and process signal strength information.

4.2.2 Performance Issues

The performance issues that were considered during the design of the modem controller software were the timing requirements that must be met in order for the modem to process the data received over a meteor burst link and respond on the same meteor trail. These requirements vary with data rate and message size.

As the data rate increases, the time available for processing the received data decreases, since the interrupts occur at a higher frequency. Table 4.2.2-1 shows the relationship between data rate and the time between transmit and receive interrupts.

Data Rate	Time Between Interrupts	
	Transmit Interrupts	Receive Interrupts
4 kbps	28.00 msec	32.0 msec
8 kbps	14.00 msec	16.0 msec
16 kbps	7.00 msec	8.0 msec
32 kbps	3.50 msec	4.0 msec
64 kbps	1.75 msec	2.0 msec
128 kbps	0.875 msec	1.0 msec
256 kbps	0.438 msec	0.5 msec
512 kbps	0.22 msec	0.5 msec

Table 4.2.2-1 Interrupt Times for Each Data Rate

During the development phase, problems were encountered in meeting the transmit interrupt timing requirements at the highest data rates. One of those requirements is the need to keep the transmit FIFO loaded with data. As discussed in section 3.2.4, this is necessary to ensure that there are no gaps in the transmit data stream. The time required to load the transmit FIFO varies depend on what routine the modem controller is processed

when the interrupt occurs. Under worst case conditions, the processor had difficulty loading the transmit FIFO within the allotted time when operating at the 512 kbps data rate. This problem was resolved by adding a programmable counter to the transmit/receive baseband boards, which keeps track of the number of bytes of data left in the transmit FIFO. The programmable counter interrupts the processor when one byte is left in the FIFO instead of when the FIFO is transferring the last byte. This change allows the processor to load the transmit FIFO within the allotted time when operating at all data rates.

Another problem encountered during the development phase was optimizing the software design so that the controller would have sufficient time to process the receive data when operating at the higher data rates. One area that was investigated to determine its effect on the receive processing time was adjusting the amount of data stored in the transmit and receive FIFO's. With transmit interrupts occurring every 0.22 msec, if the receive interrupts occur too often, very little time remains for processing the received data between interrupts. While increasing the amount of data stored in the transmit FIFO increases the time between transmit interrupts, tests showed that this had little effect on the receive processing capability. However, doubling the number of bytes stored in the receive FIFO when going from 256 to 512 kbps did improve the receive processing capability at 512 kbps.

One method of increasing the program execution speed was to minimize the amount of code the program has to execute when it is receiving and processing data. Figure 4.2.1-1 shows the program flow during this mode of operation. The routines shown within the dotted outline are the time critical processes in the modem software. Any interrupts that occur within these routines, affect the timing required to process the received data and load new data into the transmit buffer.

As shown in the flow diagram, when the modem powers up, the software initializes the software variables and sets up the communications and Reed Solomon hardware to the default settings. Once this is completed and the modem begins transmitting, the program checks to see if there is a command from the control terminal. If no command has been received, it then checks to see if the transmitter is still enabled and the modem is receiving data. The program stays in this loop until either a command from the control terminal is received or the receive data processing routine indicates that the link has been lost. While processing the receive data, the transmit routine is called whenever conditions indicate that new data needs to be loaded into transmit buffer.

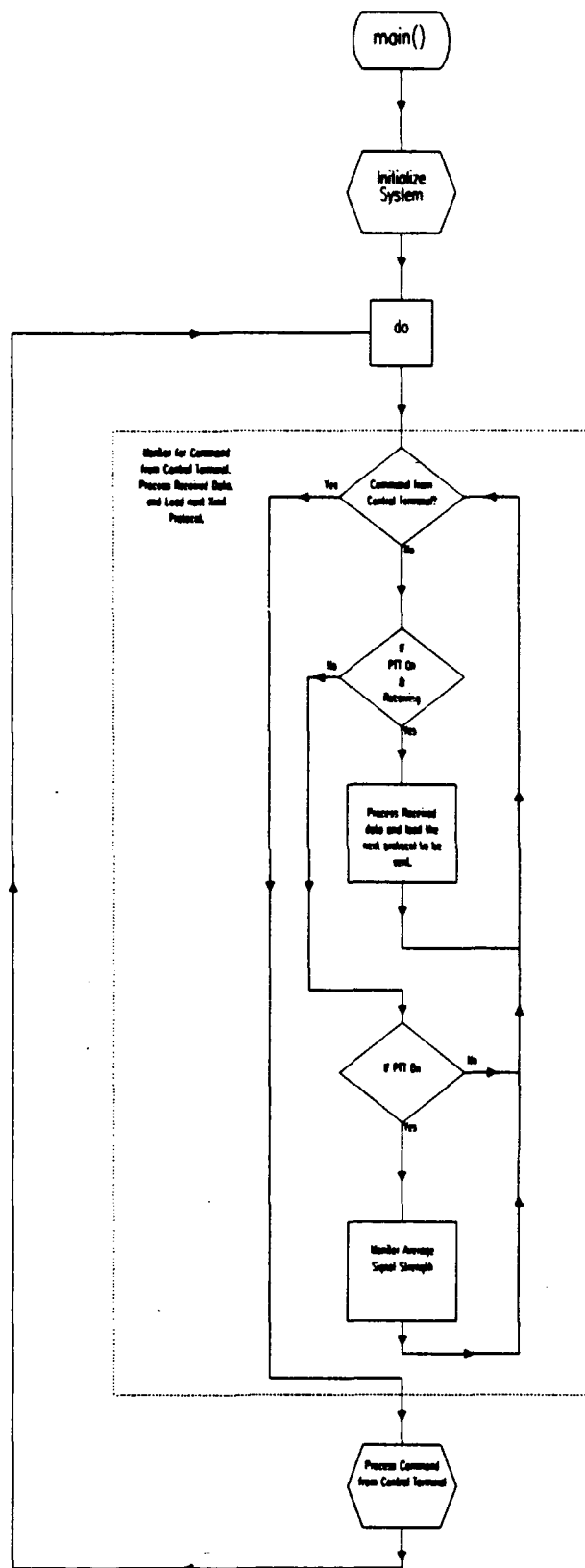


Figure 4.2.2-1 Flow Diagram Showing the Critical Timing Processes

When the transmitter is enabled and the modem is searching for a link, the program monitors the average signal strength of the station until either a command is received from the control terminal to disable the transmitter or data has been received.

Once a link is established, the Received Data Handler routine determines what information was received and what it should receive next (what type of control frame or data packet) to ensure that messages are received and transmitted as efficiently as possible.

When the Received Data Handler verifies that sufficient data is in the buffer for the expected protocol type, the data is read out and processed according to the expected data type. The next data type (control frame or data packet) to be sent is determined by the Transmit Protocol Routine. The Received Data Handler calls this routine when it determines the a new data type should be transmitted.

A link is declared lost when uncorrected errors in two consecutive data packets or control frames are detected back to back in the received data. At this point, the modem controller is set up again to probe for a meteor burst link.

REFERENCES

- [1] F. Akram, "Impulse Response of a Meteor Burst Communication Channel Determined by Ray Tracing Techniques," *IEEE Trans. on Communications*, pp. 467-470, April 1977.
- [2] Briefing given by Meteor Communications Corp. (MCC) during a visit to their facility in 1991.
- [3] ITT-A/CD, *Meteor Burst Communications Improvement Study Design Plan*, ELIN No. A002 of Contract No. F30602-89-C-0024, 27 November 1989.
- [4] ITT-A/CD, *Meteor Burst Communications Improvement Study Design Plan*, ELIN No. A002, pp. 45-91, 27 November 1989.
- [5] M. B. Pursley, "Variable-Rate Coding for Meteor-Burst Communications," *IEEE Transactions on Communications*, Vol. 37, No. 11, pp. 1105-1112, November 1989.
- [6] ITT-A/CD, *Meteor Burst Modem Operator's Manual*, ELIN No. A006 of Contract No. F30602-89-C-0024, 11 December 1990.
- [7] C. M. Chie, "Performance Analysis of Digital Integrate-and-Dump Filters," *IEEE Transactions on Communications*, Vol. 30, No. 8, pp. 1979-1983, August 1982.
- [8] J. Millman and H. Taub, *Pulse, Digital, and Switching Waveforms*, McGraw-Hill Inc., pp. 34.
- [9] R. C. Tausworthe, "Simplified Formula for Mean Cycle-Slip Time of Phase-Locked Loops With Steady-State Phase Error," *IEEE Transactions on Communication*, Vol. COM-20, pp. 331-337, June 1972.

APPENDIX A

BOARD LAYOUT & SCHEMATICS

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Slot 3 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DS1*	A12
DS0*	A13
WRITE*	A14
GND	A15
DTACK*	A16
GND	A17
AS*	A18
GND	A19
LACK*	A20
LACKIN*	A21
LACKOUT*	A22
AM4	A23
A07	A24
A06	A25
A05	A26
A04	A27
A03	A28
A02	A29
A01	A30
-12V	A31
+5V	A32
BRST*	B1
BCLR*	B2
ACFAIL*	B4
BG0IN*	B5
BG0OUT*	B6
BG1IN*	B7
BG1OUT*	B8
BG2IN*	B9
BG2OUT*	B10
BG3IN*	B11
BG3OUT*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SERCLK (1)	B21
SERDAT (1)	B22
GND	B23
IR07*	B24
IR06*	B25
IR05*	B26
IR04*	B27
IR03*	B28
IR02*	B29
IR01*	B30
+5VETDRY	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
SERR*	C11
SYSRESET*	C12
LWORD*	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

VME-J1

SLOT A03

A1	GND
A2	0 SIGNAL OUT
A3	0 SIGNAL OUT
A4	
A5	
A6	TA DATA
A7	
A8	
A9	
A10	GND
A11	TA PREO DATA
A12	TA PREO DATA
A13	TA PREO DATA
A14	TA PREO DATA
A15	TA PREO DATA
A16	TA PREO CLK
A17	TA PREO CLK
A18	GND
A19	
A20	
A21	VCA DATA
A22	GND
A23	
A24	
A25	TUNER ENA
A26	
A27	
A28	
A29	
A30	GND
A31	+5V
A32	+5V
B1	+5V
B2	GND
B3	
B4	
B5	
B6	
B7	
B8	
B9	
B10	
B11	
B12	GND
B13	+5V
B14	
B15	
B16	
B17	
B18	
B19	
B20	
B21	
B22	GND
B23	
B24	
B25	
B26	
B27	
B28	
B29	
B30	
B31	GND
B32	+5V
C1	
C2	GND
C3	
C4	
C5	
C6	
C7	
C8	
C9	
C10	GND
C11	
C12	
C13	
C14	FS
C15	FS0
C16	FS1
C17	GND
C18	SIG STR OUT
C19	
C20	
C21	
C22	GND
C23	SIG STR
C24	
C25	
C26	
C27	SC CLK
C28	
C29	
C30	GND
C31	+5V
C32	+5V

RF ASSEMBLY CONNECTION
VME-J2

Slot 4 VME J1 & J2 Connector

SLOT A12-A1

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DS1*	A12
DS0*	A13
WRITE*	A14
GND	A15
DTACK*	A16
GND	A17
AS*	A18
GND	A19
IACK*	A20
IACKIN*	A21
IACKOUT*	A22
AM4	A23
A07	A24
A06	A25
A04	A26
A03	A27
A02	A28
A01	A29
-12V	A30
+5V	A31
BBY*	B1
BCLA*	B2
ACFAIL*	B3
BG0IN*	B4
BG0OUT*	B5
BG1IN*	B6
BG1OUT*	B7
BG2IN*	B8
BG2OUT*	B9
BG3IN*	B10
BG3OUT*	B11
BR0*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SERCLK (1)	B21
SERDAT (1)	B22
GND	B23
IRQ0*	B24
IRQ1*	B25
IRQ2*	B26
IRQ3*	B27
IRQ4*	B28
IRQ5*	B29
IRQ6*	B30
+5VSTBY	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
BERR*	C11
SYSRESET*	C12
LNORD*	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

VME-J1

SLOT A04

A1	GND
A2	RA DATA IO
A3	RA DATA IN
A4	RA DATA OUT
A5	RA FIFO EP
A6	RA
A7	RA
A8	RA
A9	RA
A10	RA
A11	RA DATA RES
A12	RA DATA
A13	RA CLK
A14	RA RESET
A15	RA
A16	GND
A17	GND
A18	MOD SEL A
A19	MOD SEL A
A20	MOD SEL A
A21	MOD SEL A
A22	GND
A23	GND
A24	RA DATA
A25	RA DATA
A26	RA DATA
A27	RA DATA
A28	RA DATA
A29	RA DATA
A30	GND
A31	+5V
A32	+5V
B1	+5V
B2	GND
B3	GND
B4	GND
B5	GND
B6	GND
B7	GND
B8	A28
B9	A29
B10	A28
B11	A29
B12	GND
B13	+5V
B14	+5V
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
B22	GND
B23	GND
B24	GND
B25	GND
B26	GND
B27	GND
B28	GND
B29	GND
B30	GND
B31	GND
B32	+5V
C1	GND
C2	GND
C3	GND
C4	STATE RD
C5	STATE RD
C6	STATE RD
C7	STATE RD
C8	STATE RD
C9	STATE RD
C10	GND
C11	GND
C12	GND
C13	GND
C14	GND
C15	GND
C16	GND
C17	GND
C18	GND
C19	GND
C20	GND
C21	GND
C22	GND
C23	GND
C24	GND
C25	GND
C26	GND
C27	GND
C28	GND
C29	GND
C30	GND
C31	+5V
C32	+5V

FRG. FIFO
VME-J2

Slot 5 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DS1*	A12
DS0*	A13
WRITE*	A14
GND	A15
DTACK*	A16
GND	A17
AS*	A18
GND	A19
LACK*	A20
LACKIN*	A21
LACKOUT*	A22
AMA	A23
A07	A24
A06	A25
A05	A26
A03	A27
A02	A28
A01	A29
-12V	A30
+5V	A31
BBSV*	B1
BCLK*	B2
ACFAIL*	B3
BG0IN*	B4
BG0OUT*	B5
BG1IN*	B6
BG1OUT*	B7
BG2IN*	B8
BG2OUT*	B9
BG3IN*	B10
BG3OUT*	B11
BR0*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SENCLK (1)	B21
SENDAT* (1)	B22
GND	B23
IRQ7*	B24
IRQ6*	B25
IRQ5*	B26
IRQ4*	B27
IRQ3*	B28
IRQ2*	B29
IRQ1*	B30
+5VSTD	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
BERR*	C11
SYSRESET*	C12
LNORD*	C13
AMS	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

VME-J1

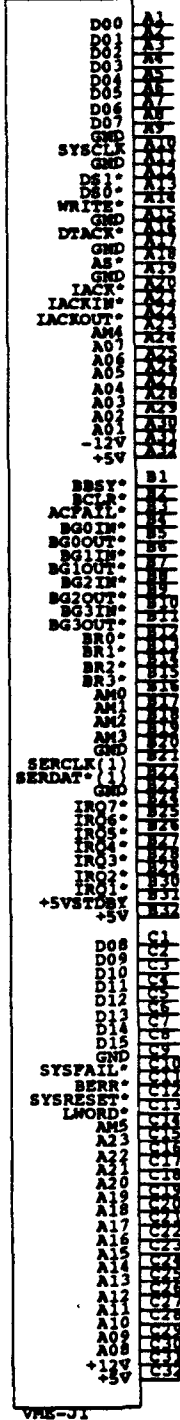
SLOT A05

A1	GND
A2	DEP00 RESET*
A3	DEP01 SEC*
A4	W-ARY SEL
A5	SA* SYNC EN
A6	DATA FARE STATE
A7	INV CLK OUT CLK
A8	SUM DATA CLK
A9	INV SUM DATA CLK
A10	GND
A11	CC DATA CLK
A12	INV CC DATA CLK
A13	PCO CLK
A14	PCI CLK
A15	ACQ/TRA-N
A16	RESET*
A17	NON SECT A
A18	CORR CLK
A19	SIN SYNC CLK
A20	PSK SEL
A21	IS SEI RES CLK
A22	GND
A23	RAM RSACK
A24	ROTATE CLK
A25	DATA SUM LATCH CLK-N
A26	ACQIN PAUSE CLK
A27	ACQIN PAUSE CLK
A28	SYN SUM PAUSE CLK
A29	SYN LATCH CLK
A30	GND
A31	+5V
A32	+5V
B1	+5V
B2	GND
B3	SYN LATCH CLK-N
B4	PAR/SEK SEV/IN-X
B5	R-ARY DATA CLK
B6	SYN DET-N
B7	EXACT CLK COM
B8	RAW CLK COM
B9	MOD SPAN COM
B10	TRIG OUT
B11	TRIG IN
B12	GND
B13	+5V
B14	TRIG ON
B15	TRIG RESET-N
B16	TRIG DATA SEL
B17	IN ENABLE
B18	IN RESET
B19	IN SECT
B20	EVEN CORR CLK
B21	ODD CORR CLK
B22	GND
B23	RES-ON
B24	INVEN/ODD SEL
B25	DATA END
B26	RAM OR-N
B27	RAM WR-N
B28	SH/ROX-N
B29	DATA
B30	RAM ADDR V
B31	GND
B32	+5V
C1	GND
C2	RAM ADDR 1
C3	RAM ADDR 2
C4	RAM ADDR 3
C5	RAM ADDR 4
C6	RAM ADDR 5
C7	RAM ADDR 6
C8	RAM ADDR 7
C9	RAM ADDR 8
C10	GND
C11	GND
C12	DRN
C13	DRN
C14	CHAC DATA CLK
C15	SAMPLE CLK
C16	SPSK LO SEL-N
C17	SPSK HI SEL-N
C18	GND
C19	DPSK SEL-N
C20	PD LO SEL-N
C21	PD HI SEL-N
C22	LATCH CLK
C23	GND
C24	CHAC OUT CWRLL
C25	CHAC OUT CWRLL
C26	CHAC OUT CWRLL
C27	NCO RESET
C28	ACC/DUNE
C29	ACC CLK
C30	GND
C31	+5V
C32	+5V

TIMING
VME-J2

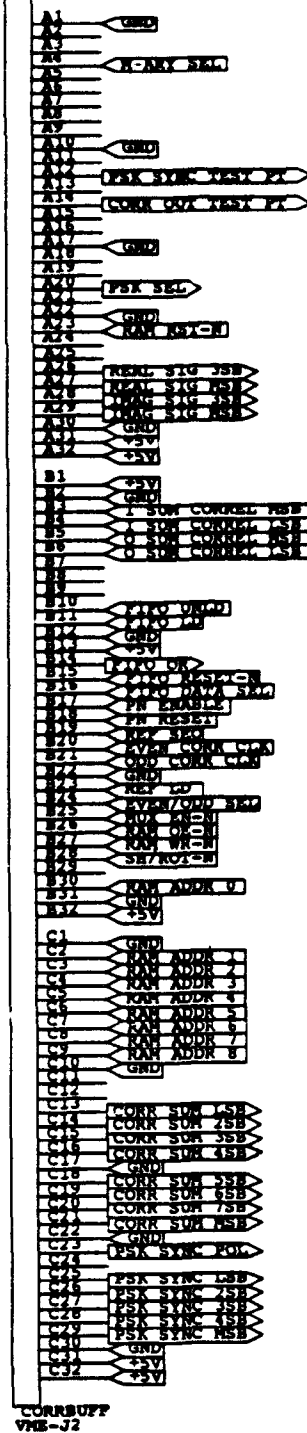
Slot 6 VME J1 & J2 Connector

SLOT A12-A01



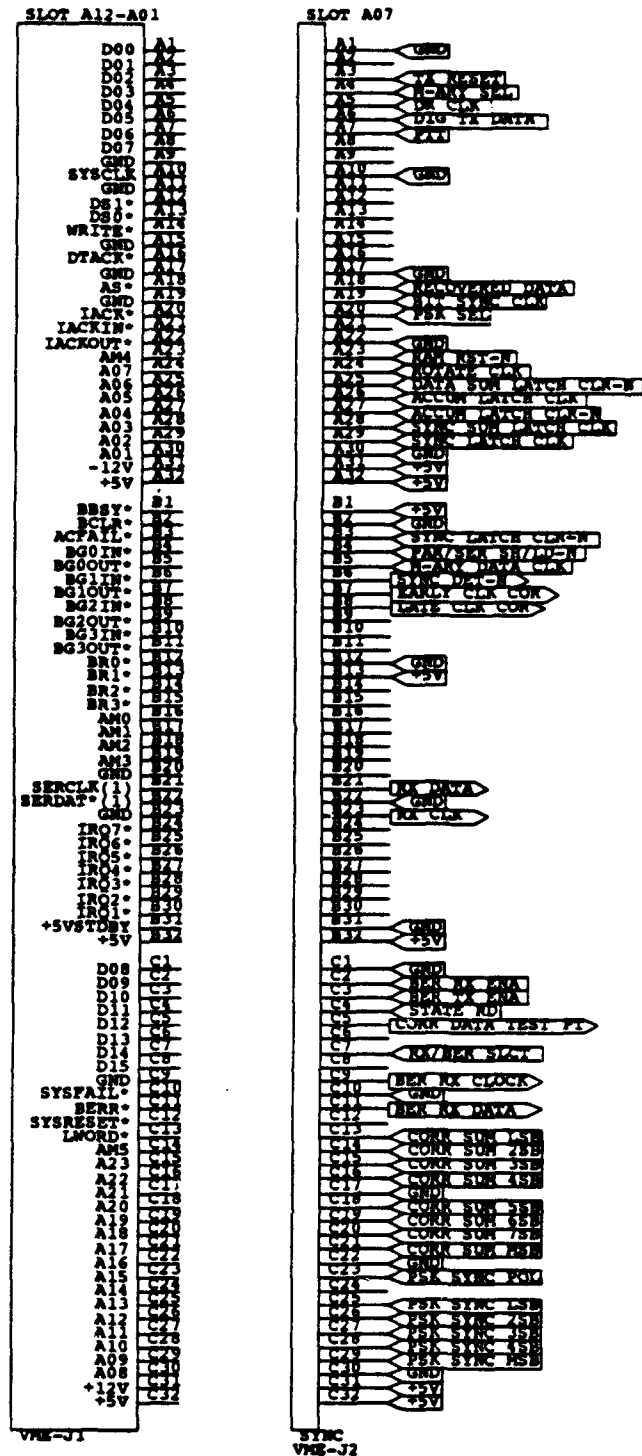
VME-J1

SLOT A06



CORRBUF
VME-J2

Slot 7 VME J1 & J2 Connector



Slot 8 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
DS1*	A11
DS0*	A12
WRITE*	A13
GND	A14
DTACK*	A15
GND	A16
AS*	A17
GND	A18
LACK*	A19
LACKIN*	A20
LACKOUT*	A21
AM4	A22
A07	A23
A06	A24
A05	A25
A04	A26
A03	A27
A02	A28
A01	A29
-12V	A30
+5V	A31
BBSV*	B1
BCL*	B2
ACTFAIL*	B3
BG0IN*	B4
BG0OUT*	B5
BG1IN*	B6
BG1OUT*	B7
BG2IN*	B8
BG2OUT*	B9
BG3IN*	B10
BG3OUT*	B11
BR0*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SENCLK(1)	B21
SENDA*(1)	B22
GND	B23
IRO7*	B24
IRO6*	B25
IRO5*	B26
IRO4*	B27
IRO3*	B28
IRO2*	B29
IRO1*	B30
+5VSTD*	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
BERR*	C11
SYSRESET*	C12
LNWORD*	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
+12V	C30
+5V	C31
	C32

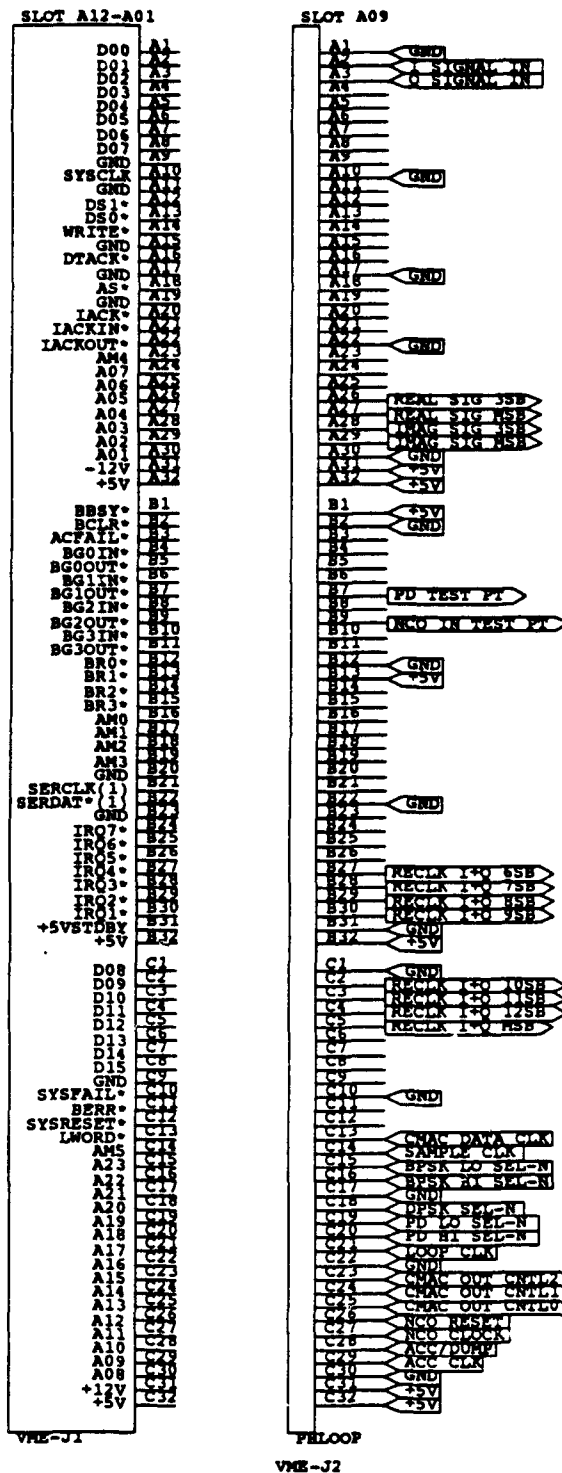
VME-J1

SLOT A08

A1	GND
A2	DECODE RESET*
A3	DESK SMD
A4	N-RAY SEL
A5	B11 SYNC SW
A6	DATA PATH SMD
A7	INV CLK VDA CLK
A8	SUN DATA CLK
A9	INV SUN DATA CLK
A10	GND
A11	CO DATA CLK
A12	INV CO DATA CLK
A13	PCO CLK
A14	PCI CLK
A15	ACV/TRK-N
A16	BASE*
A17	GND
A18	UNCOVERED DATA
A19	B11 SYNC CLK
A20	
A21	
A22	GND
A23	
A24	
A25	
A26	
A27	
A28	
A29	
A30	GND
A31	+5V
A32	+5V
B1	+5V
B2	GND
B3	I SUN CORREL. HSE
B4	O SUN CORREL. HSE
B5	O SUN CORREL. HSE
B6	O SUN CORREL. LSE
B7	
B8	
B9	O TRK TEST PT
B10	
B11	I TRK TEST PT
B12	GND
B13	+5V
B14	
B15	O DPSK TEST PT
B16	
B17	I DPSK TEST PT
B18	
B19	AO DPSK TEST PT
B20	
B21	
B22	GND
B23	
B24	
B25	
B26	RECLA I=O 65B
B27	RECLA I=O 75B
B28	RECLA I=O 85B
B29	RECLA I=O 95B
B30	RECLA I=O 105B
B31	GND
B32	+5V
C1	GND
C2	RECLA I=O 105B
C3	RECLA I=O 115B
C4	RECLA I=O 125B
C5	RECLA I=O 135B
C6	
C7	
C8	
C9	
C10	GND
C11	
C12	
C13	
C14	
C15	DPSK CO SMD-N
C16	
C17	GND
C18	
C19	
C20	
C21	
C22	GND
C23	
C24	
C25	
C26	
C27	
C28	
C29	
C30	GND
C31	+5V
C32	+5V

DATAPATH
VME-J2

Slot 9 VME J1 & J2 Connector



Slot 10 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DS1*	A12
DS0*	A13
WRITE*	A14
GND	A15
DTACK*	A16
GND	A17
AS*	A18
GND	A19
LACK*	A20
LACKIN*	A21
LACKOUT*	A22
AM4	A23
A07	A24
A06	A25
A05	A26
A04	A27
A03	A28
A02	A29
A01	A30
-12V	A31
+5V	A32
BBSY*	B1
BCLR*	B2
ACFAIL*	B3
BG0IN*	B4
BG0OUT*	B5
BG1IN*	B6
BG1OUT*	B7
BG2IN*	B8
BG2OUT*	B9
BG3IN*	B10
BG3OUT*	B11
BR0*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SERCLK(1)	B21
SERDAT*(1)	B22
GND	B23
IRQ7*	B24
IRQ6*	B25
IRQ5*	B26
IRQ4*	B27
IRQ3*	B28
IRQ2*	B29
IRQ1*	B30
+5VETDBY	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
BERR*	C11
SYSRESET*	C12
LWORD*	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

VME-J1

SLOT A10

A1	GND
A2	DMA
A3	DMA
A4	DMA
A5	DMA
A6	DM CLK
A7	MOD SELECT A
A8	MOD SELECT B
A9	P11
A10	GND
A11	CORR RESP
A12	SIG CLK-N
A13	TX DATA
A14	RX DATA
A15	GND
A16	GND
A17	GND
A18	MOD SEL
A19	GND
A20	GND
A21	GND
A22	GND
A23	GND
A24	GND
A25	GND
A26	GND
A27	TX RESET
A28	GND
A29	DIG TX DATA
A30	GND
A31	+5V
A32	+5V
B1	+5V
B2	GND
B3	GND
B4	A24
B5	A25
B6	A26
B7	A27
B8	A28
B9	A29
B10	A30
B11	A31
B12	GND
B13	+5V
B14	D16
B15	D17
B16	D18
B17	D19
B18	D20
B19	D21
B20	D22
B21	D23
B22	GND
B23	D24
B24	D25
B25	D26
B26	D27
B27	D28
B28	D29
B29	D30
B30	D31
B31	GND
B32	+5V
C1	GND
C2	RX INTR LO
C3	RX INTR HI
C4	RX INTR RES
C5	RX FIFO RT
C6	RX RESET
C7	GND
C8	RX/BER SLC
C9	BER RX CLOCK
C10	GND
C11	BER RX DATA
C12	GND
C13	GND
C14	GND
C15	GND
C16	GND
C17	GND
C18	GND
C19	GND
C20	GND
C21	GND
C22	SIG STR OUT
C23	GND
C24	SIG STR
C25	GND
C26	GND
C27	SC CLK
C28	HSC CLK
C29	70MHZ
C30	16MHZ
C31	GND
C32	+5V

BBRX
VME-J2

Slot 11 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DS1*	A12
DS0*	A13
WRITE*	A14
GND	A15
DTACK*	A16
GND	A17
AS*	A18
GND	A19
IACK	A20
IACKIN*	A21
IACKOUT*	A22
IACKOUT*	A23
AM4	A24
A07	A25
A06	A26
A05	A27
A04	A28
A03	A29
A01	A30
-12V	A31
+5V	A32
BBSY*	B1
BCLR*	B2
ACFAIL*	B3
BGOIN*	B4
BGOOUT*	B5
BGIIN*	B6
BGIOUT*	B7
BG2IN*	B8
BG2OUT*	B9
BG3IN*	B10
BG3OUT*	B11
BR0*	B12
BR1*	B13
BR2*	B14
BR3*	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SERCLK(1)	B21
SERDAT*(1)	B22
GND	B23
IN07*	B24
IN06*	B25
IN05*	B26
IN04*	B27
IN03*	B28
IN02*	B29
IN01*	B30
+5VSTDBY	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL*	C10
BERR*	C11
SYSRESET*	C12
LNORD*	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

VME-J1

SLOT A11

A1	GND
A2	DATA
A3	DATA
A4	DATA
A5	DATA
A6	DATA
A7	DATA
A8	DATA
A9	DATA
A10	DATA
A11	DATA
A12	DATA
A13	DATA
A14	DATA
A15	DATA
A16	DATA
A17	DATA
A18	DATA
A19	DATA
A20	DATA
A21	DATA
A22	DATA
A23	DATA
A24	DATA
A25	DATA
A26	DATA
A27	DATA
A28	DATA
A29	DATA
A30	DATA
A31	DATA
A32	DATA
B1	DATA
B2	DATA
B3	DATA
B4	DATA
B5	DATA
B6	DATA
B7	DATA
B8	DATA
B9	DATA
B10	DATA
B11	DATA
B12	DATA
B13	DATA
B14	DATA
B15	DATA
B16	DATA
B17	DATA
B18	DATA
B19	DATA
B20	DATA
B21	DATA
B22	DATA
B23	DATA
B24	DATA
B25	DATA
B26	DATA
B27	DATA
B28	DATA
B29	DATA
B30	DATA
B31	DATA
B32	DATA
C1	DATA
C2	DATA
C3	DATA
C4	DATA
C5	DATA
C6	DATA
C7	DATA
C8	DATA
C9	DATA
C10	DATA
C11	DATA
C12	DATA
C13	DATA
C14	DATA
C15	DATA
C16	DATA
C17	DATA
C18	DATA
C19	DATA
C20	DATA
C21	DATA
C22	DATA
C23	DATA
C24	DATA
C25	DATA
C26	DATA
C27	DATA
C28	DATA
C29	DATA
C30	DATA
C31	DATA
C32	DATA

VME-J2

Slot 12 VME J1 & J2 Connector

SLOT A12-A01

D00	A1
D01	A2
D02	A3
D03	A4
D04	A5
D05	A6
D06	A7
D07	A8
GND	A9
SYSCLK	A10
GND	A11
DE1	A12
DE0	A13
WRITE	A14
GND	A15
DTACK	A16
GND	A17
AS	A18
GND	A19
IACK	A20
IACKIN	A21
IACKOUT	A22
AM4	A23
A07	A24
A06	A25
A05	A26
A04	A27
A03	A28
A02	A29
A01	A30
-12V	A31
+5V	A32
BBV	B1
BCLK	B2
ACTAIL	B3
BG0IN	B4
BG0OUT	B5
BG1IN	B6
BG1OUT	B7
BG2IN	B8
BG2OUT	B9
BG3IN	B10
BG3OUT	B11
BR0	B12
BR1	B13
BR2	B14
BR3	B15
AM0	B16
AM1	B17
AM2	B18
AM3	B19
GND	B20
SERCLK(1)	B21
SERDAT(1)	B22
GND	B23
IR07	B24
IR06	B25
IR05	B26
IR04	B27
IR03	B28
IR02	B29
IR01	B30
+5VSTBY	B31
+5V	B32
D08	C1
D09	C2
D10	C3
D11	C4
D12	C5
D13	C6
D14	C7
D15	C8
GND	C9
SYSFAIL	C10
BERR	C11
SYSRESET	C12
LNWORD	C13
AM5	C14
A23	C15
A22	C16
A21	C17
A20	C18
A19	C19
A18	C20
A17	C21
A16	C22
A15	C23
A14	C24
A13	C25
A12	C26
A11	C27
A10	C28
A09	C29
A08	C30
+12V	C31
+5V	C32

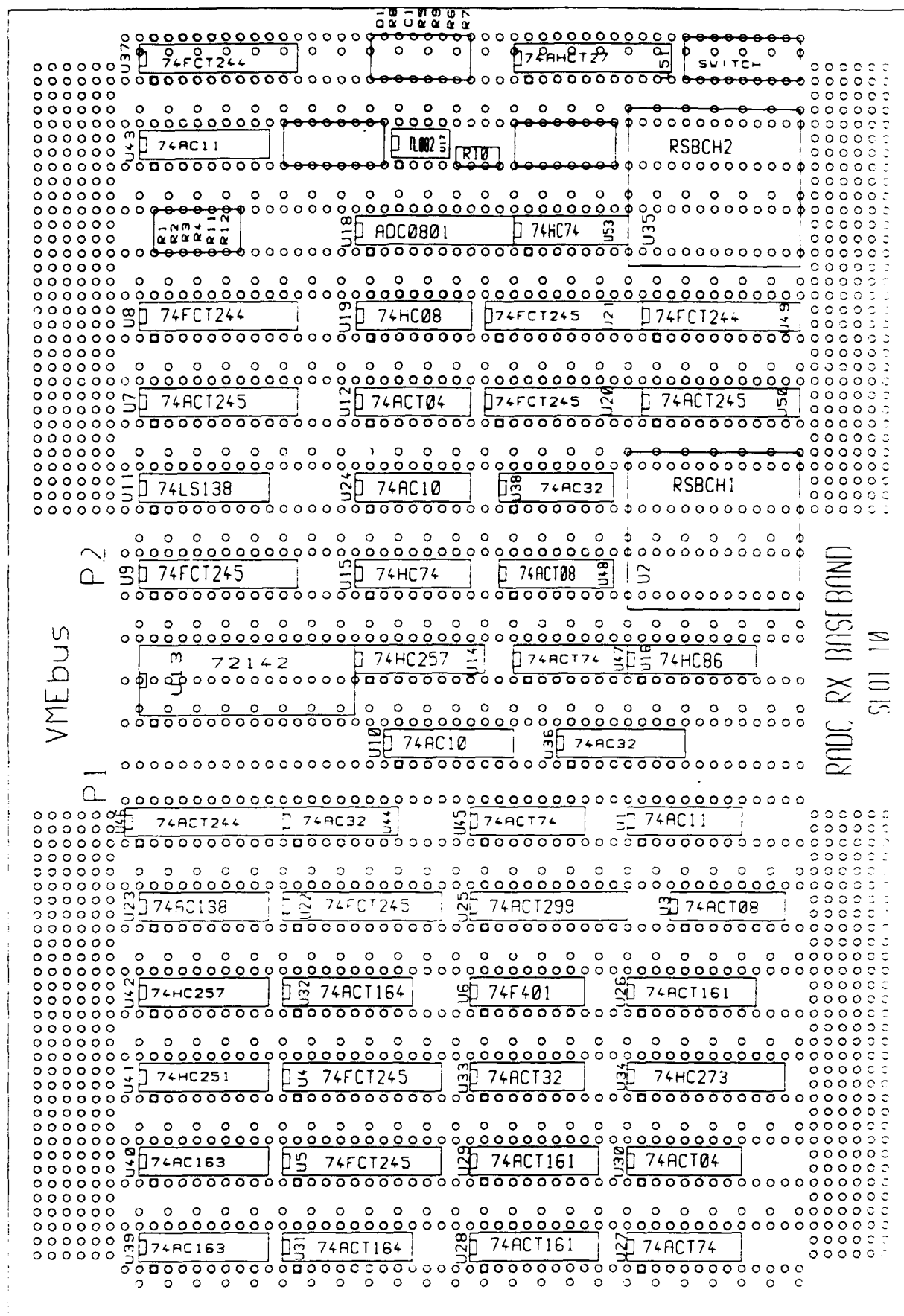
VME-J1

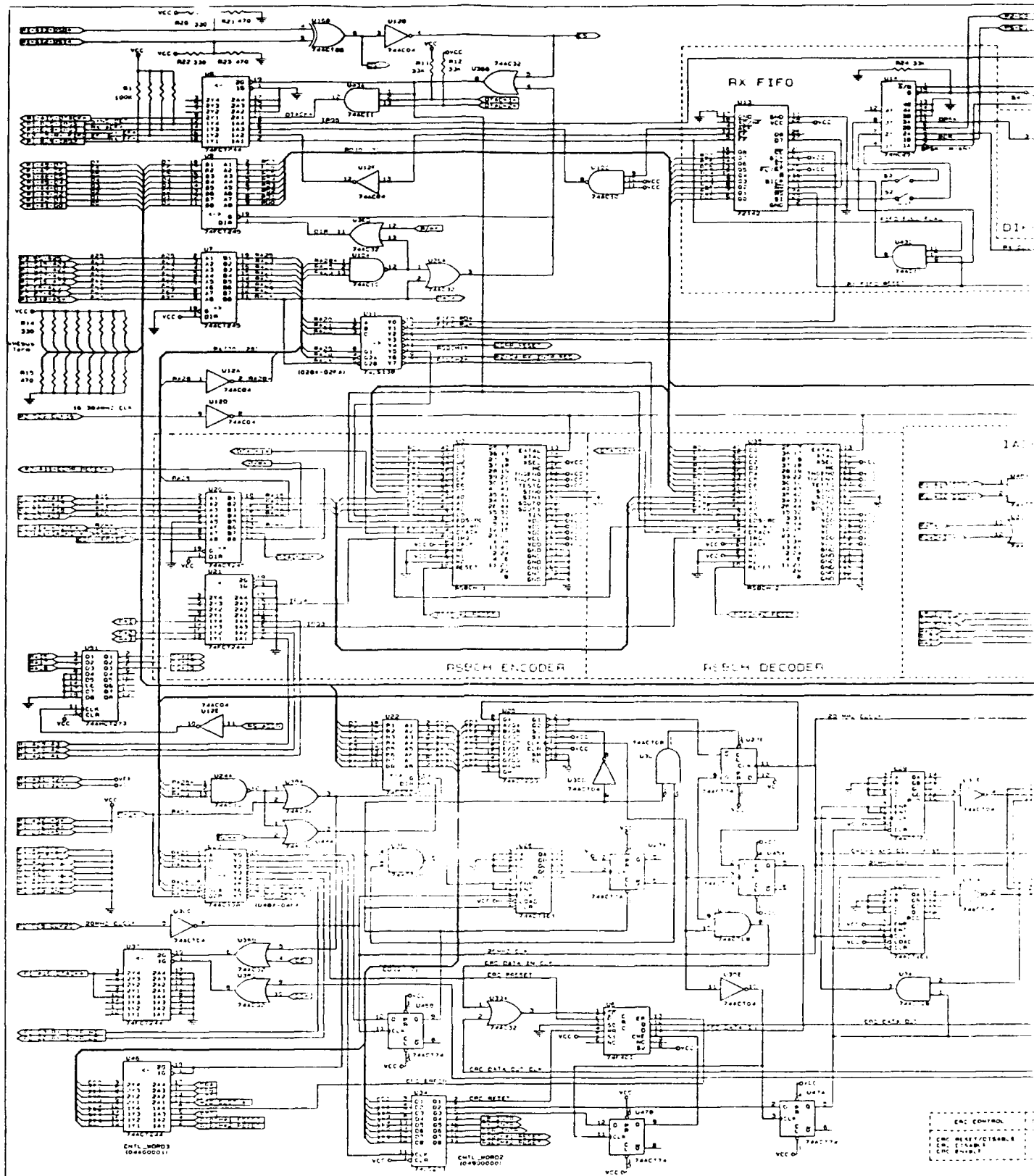
SLOT A12

A1	GND
A2	PC0
A3	PC1
A4	PC2
A5	PC3
A6	PC4
A7	PC5
A8	PC6
A9	PC7
A10	PC8
A11	PC9
A12	PC10
A13	PC11
A14	PC12
A15	PC13
A16	PC14
A17	PC15
A18	PC16
A19	PC17
A20	PC18
A21	PC19
A22	PC20
A23	PC21
A24	PC22
A25	PC23
A26	PC24
A27	PC25
A28	PC26
A29	PC27
A30	PC28
A31	PC29
A32	PC30
B1	+5V
B2	GND
B3	PC31
B4	PC32
B5	PC33
B6	PC34
B7	PC35
B8	PC36
B9	PC37
B10	PC38
B11	PC39
B12	PC40
B13	PC41
B14	PC42
B15	PC43
B16	PC44
B17	PC45
B18	PC46
B19	PC47
B20	PC48
B21	PC49
B22	PC50
B23	PC51
B24	PC52
B25	PC53
B26	PC54
B27	PC55
B28	PC56
B29	PC57
B30	PC58
B31	PC59
B32	PC60
C1	GND
C2	PC61
C3	PC62
C4	PC63
C5	PC64
C6	PC65
C7	PC66
C8	PC67
C9	PC68
C10	PC69
C11	PC70
C12	PC71
C13	PC72
C14	PC73
C15	PC74
C16	PC75
C17	PC76
C18	PC77
C19	PC78
C20	PC79
C21	PC80
C22	PC81
C23	PC82
C24	PC83
C25	PC84
C26	PC85
C27	PC86
C28	PC87
C29	PC88
C30	PC89
C31	PC90
C32	PC91

SBC
VME-J2



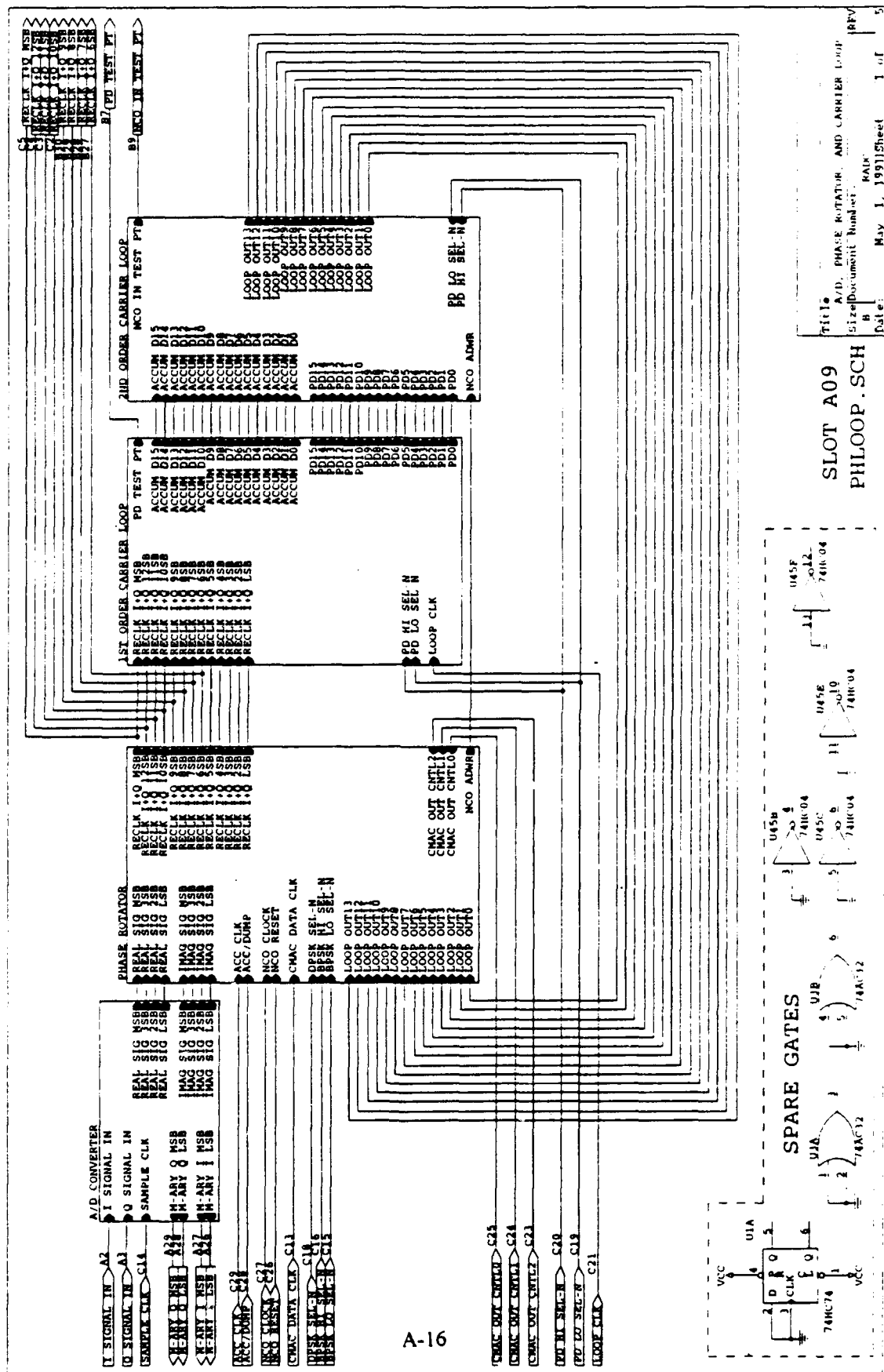




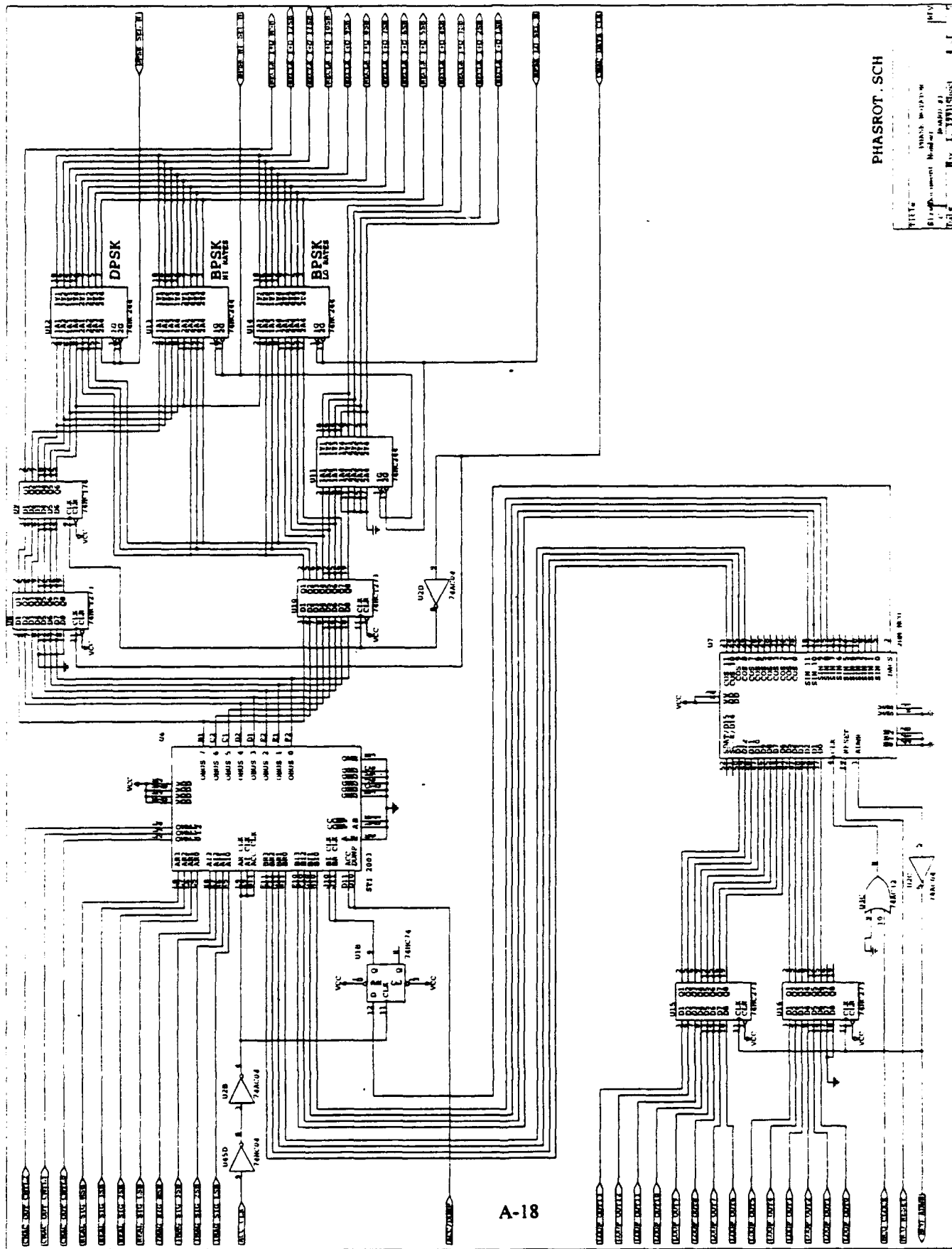
10/3

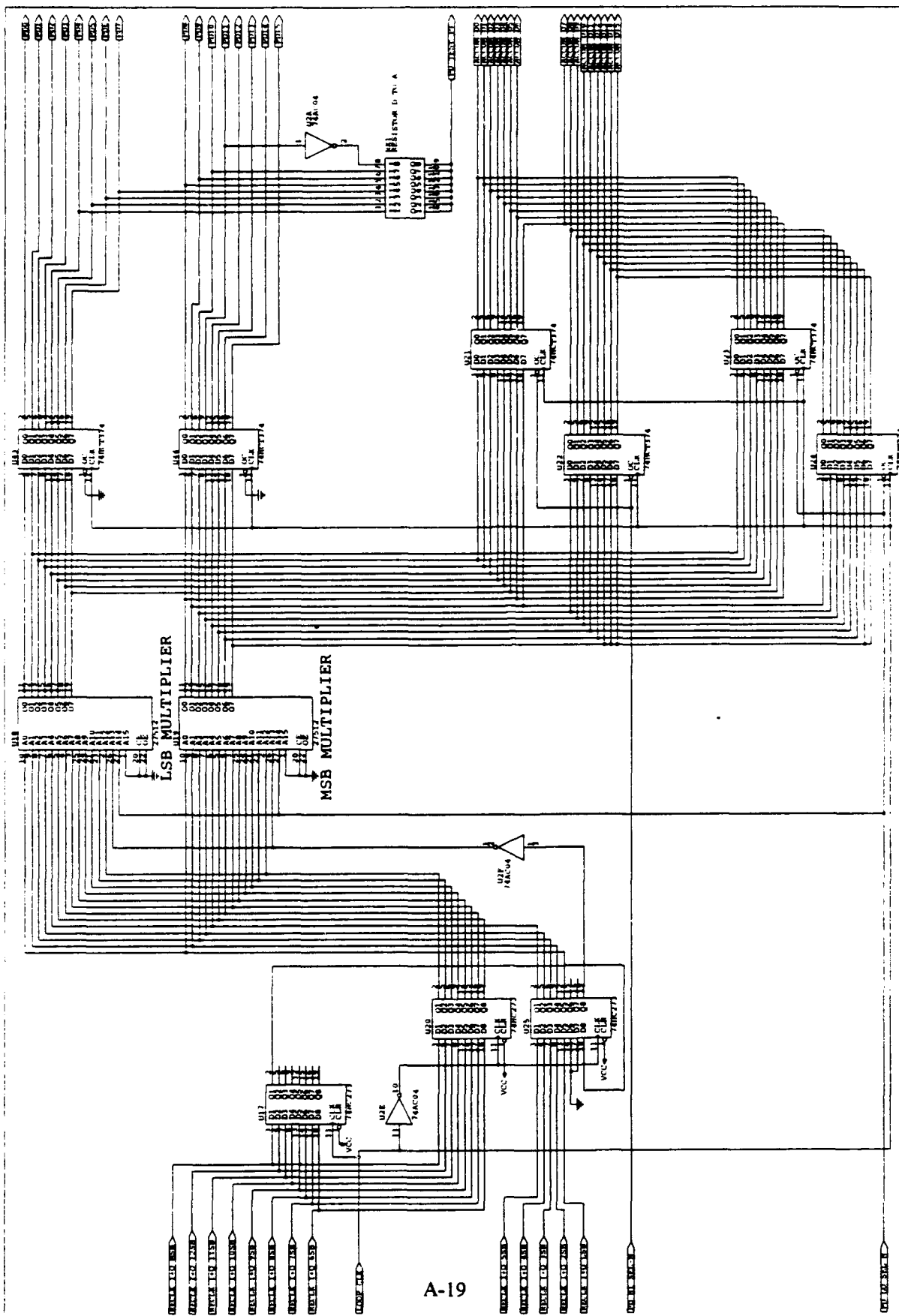








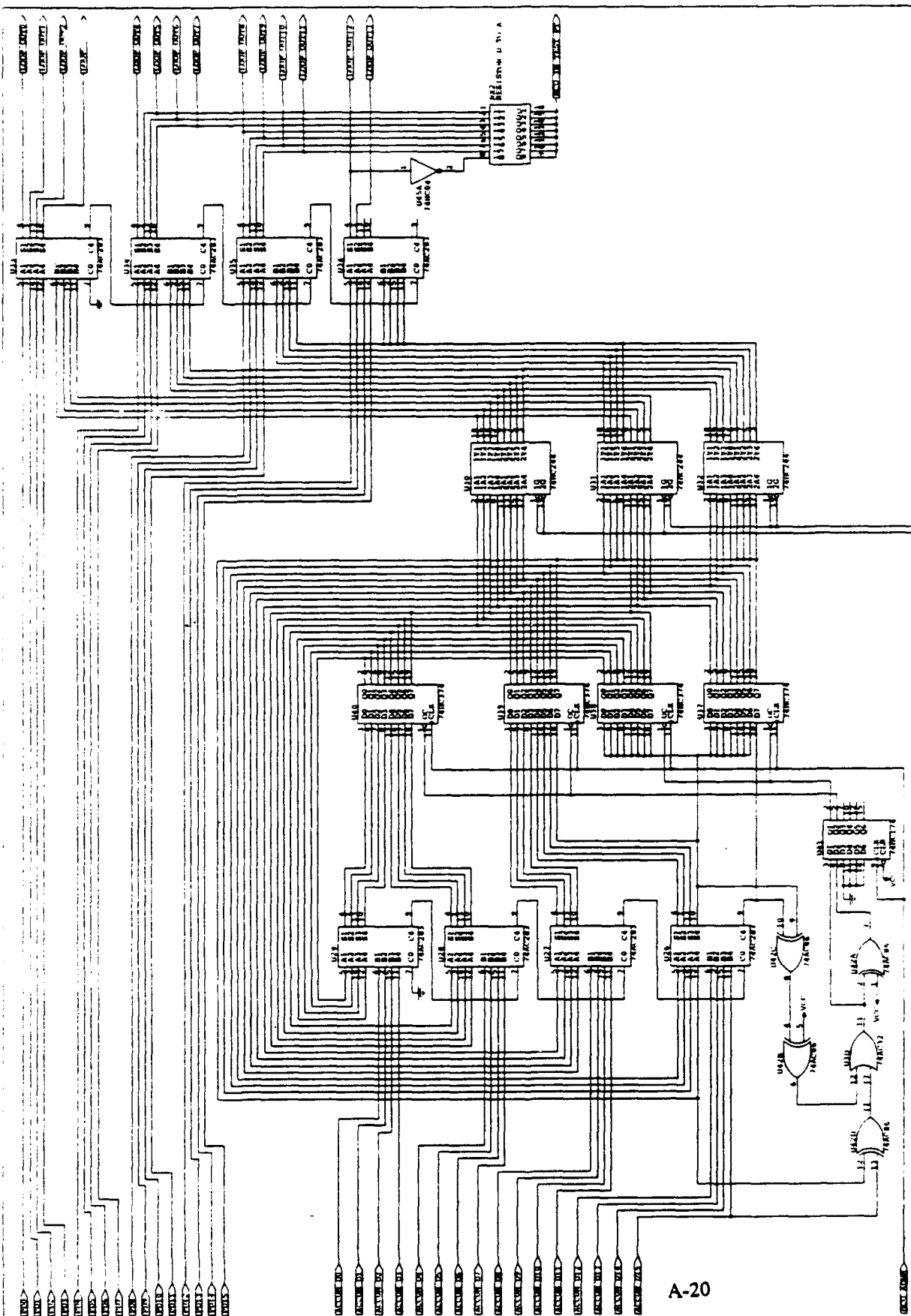




A-19

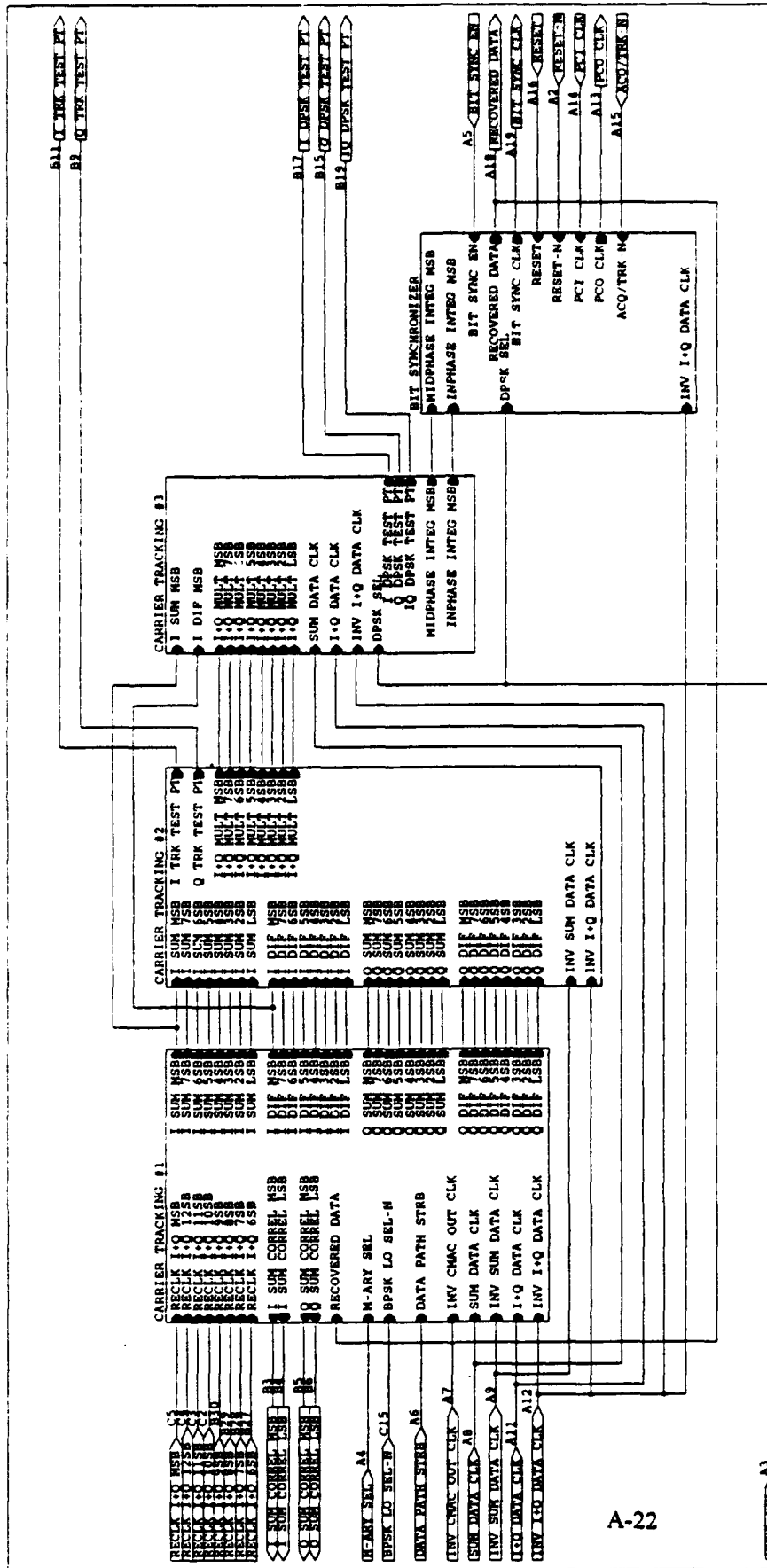
CAR_LOOP.SCH

FILE: C:\PROJ\CAR_LOOP.SCH
 SHEET: 1 OF 1
 REV: 1.00
 DATE: 11/11/93



Title:
 Date:
 Author:
 Rev:
 Part:

CARLOP2.SCH



A-22

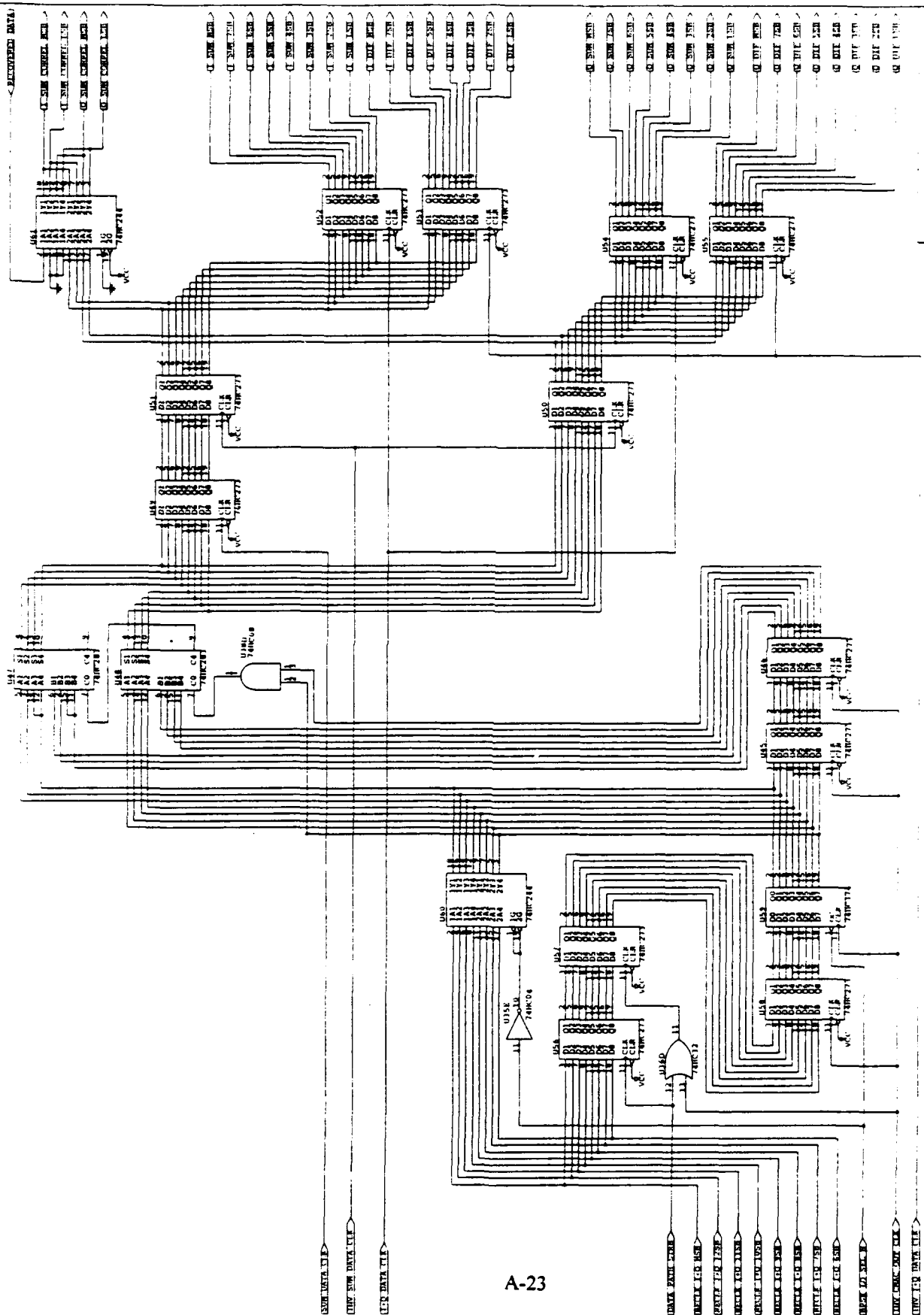
SLOT A08 DATAPATH.SCH

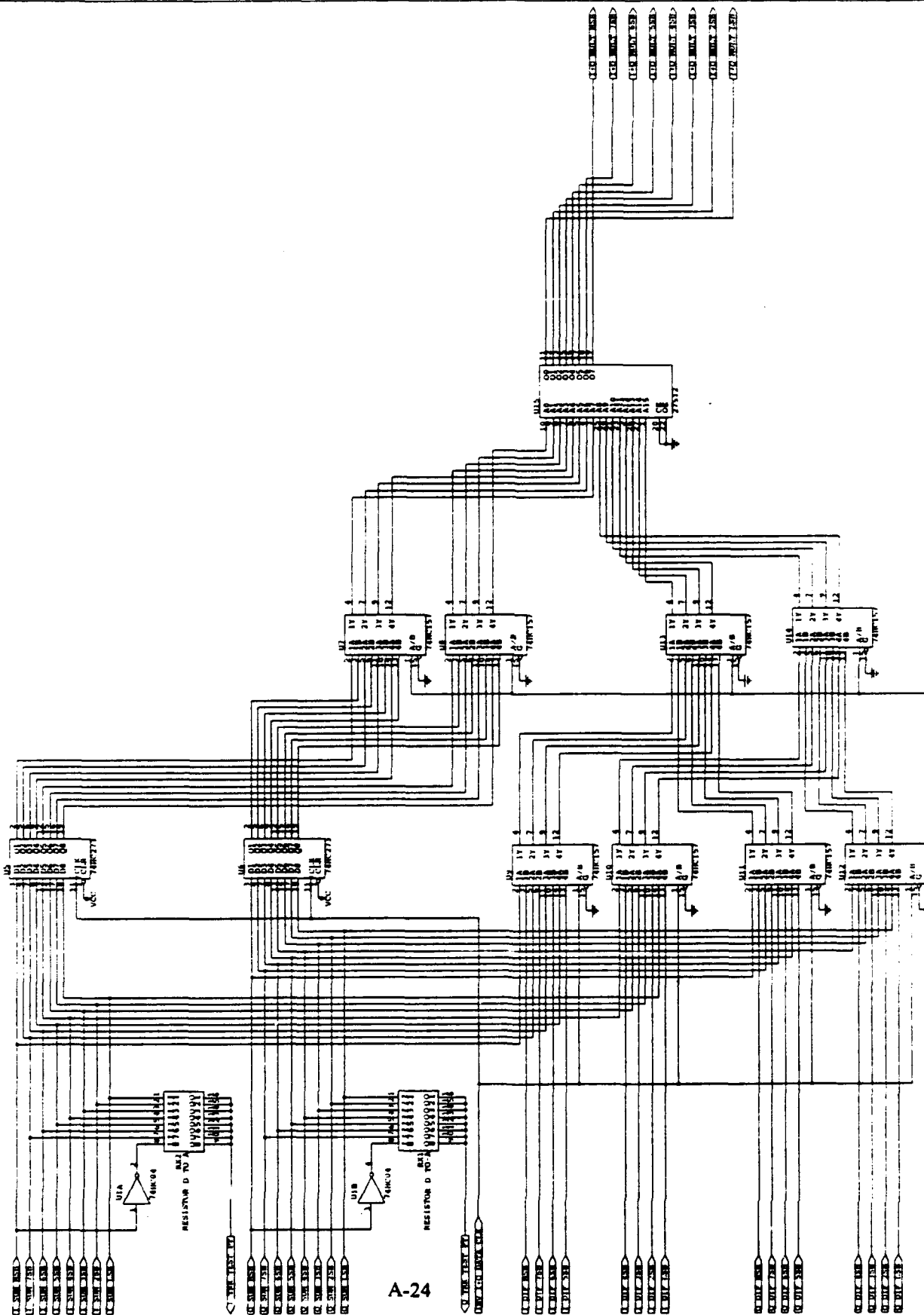
TITLE: CARRIER TRACKING AND BIT SYNC
 SIZE: 8
 DATE: February 11, 1993
 REV: 5

CARTRK.SCH

REV. 1.00
 DATE: 05/19/77
 BY: J. J. JONES

5 1 9

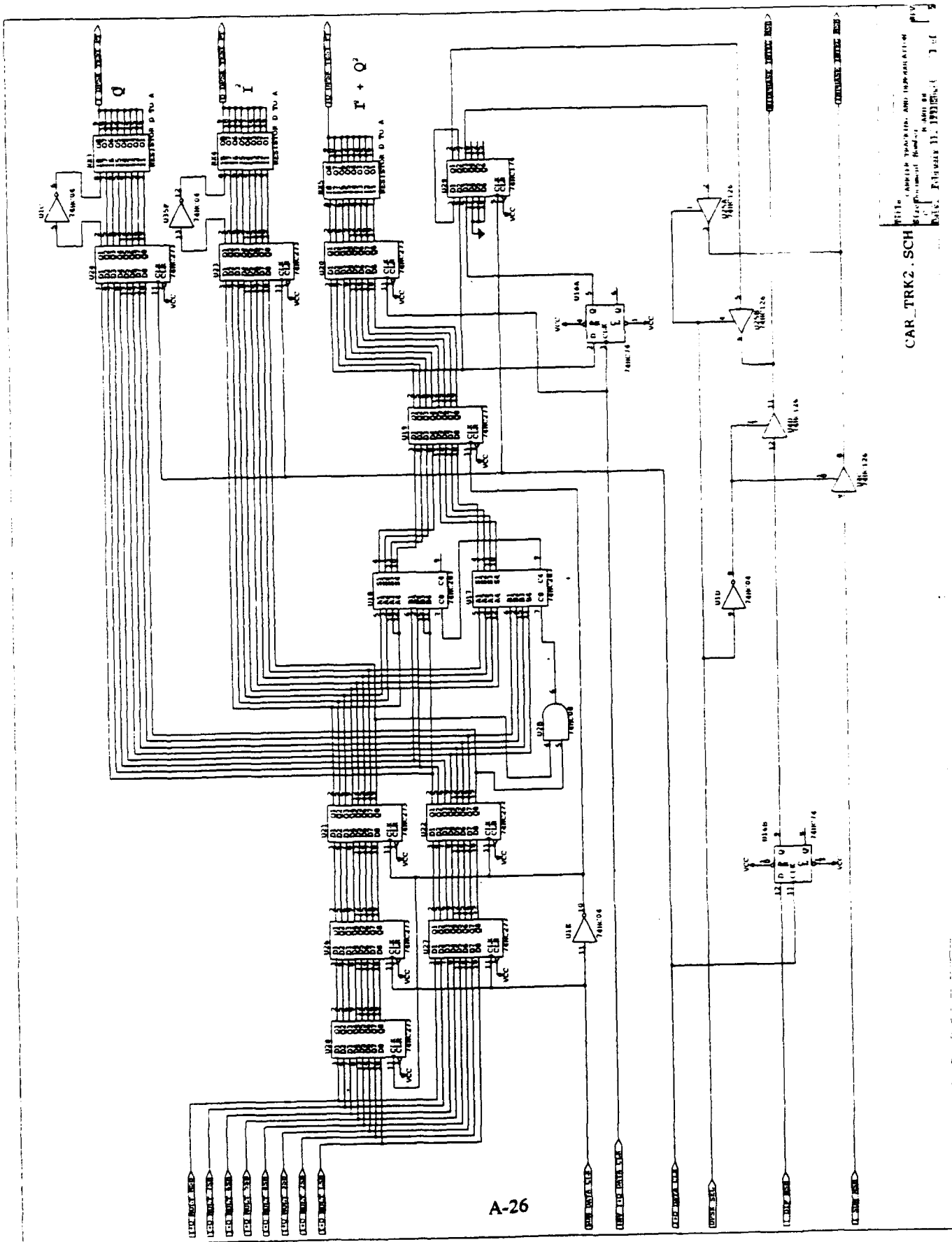




CAR_TRK1.SCH

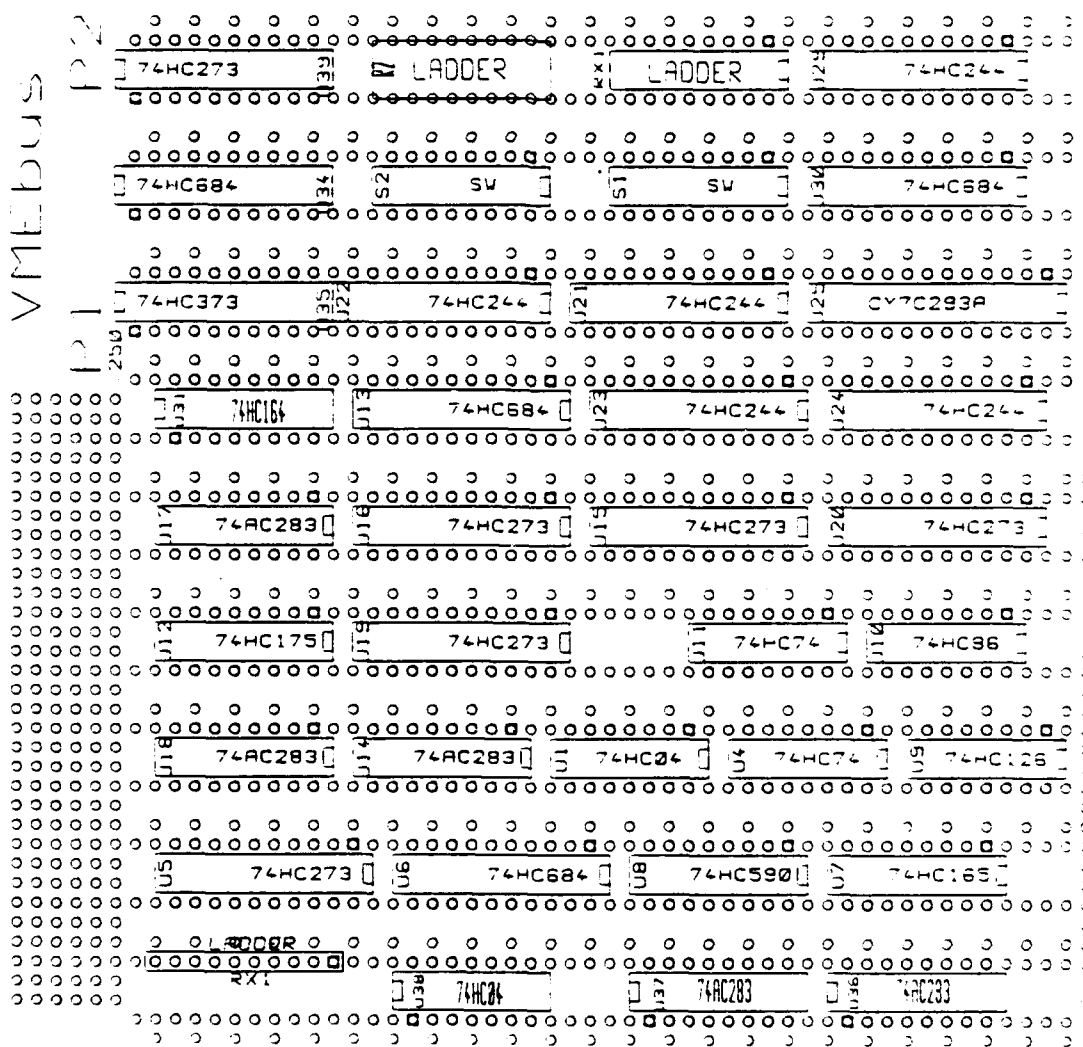
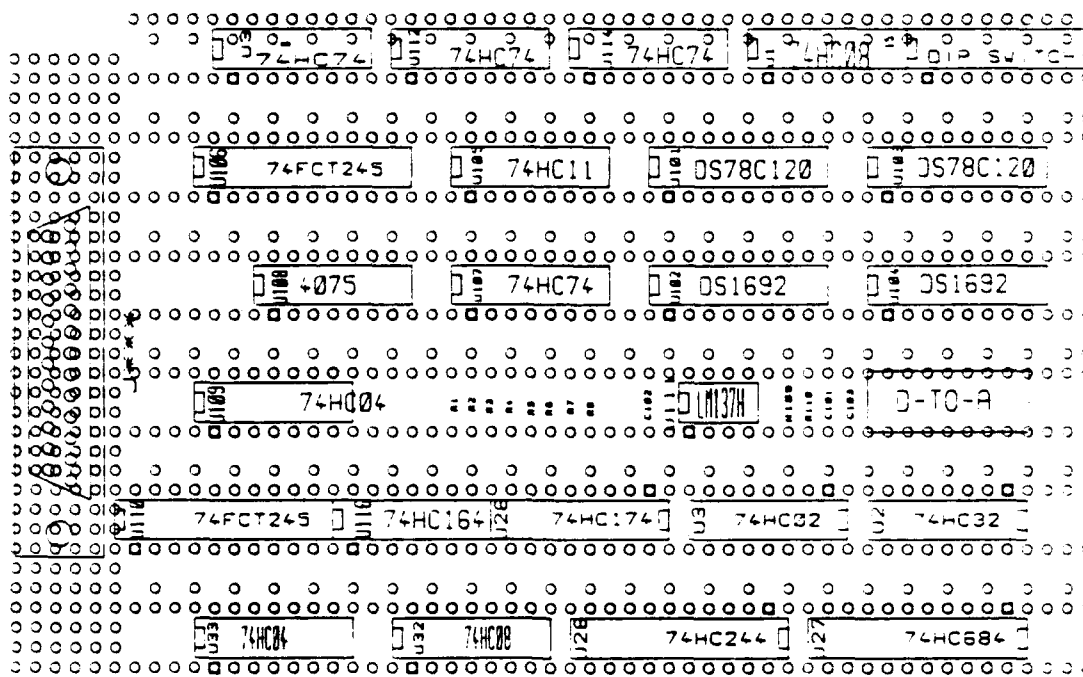
DATE: February 11, 1991
 BY: [Signature]
 CHECKED BY: [Signature]
 APPROVED BY: [Signature]
 TITLE: CAR TRK1: ADD INFORMATION

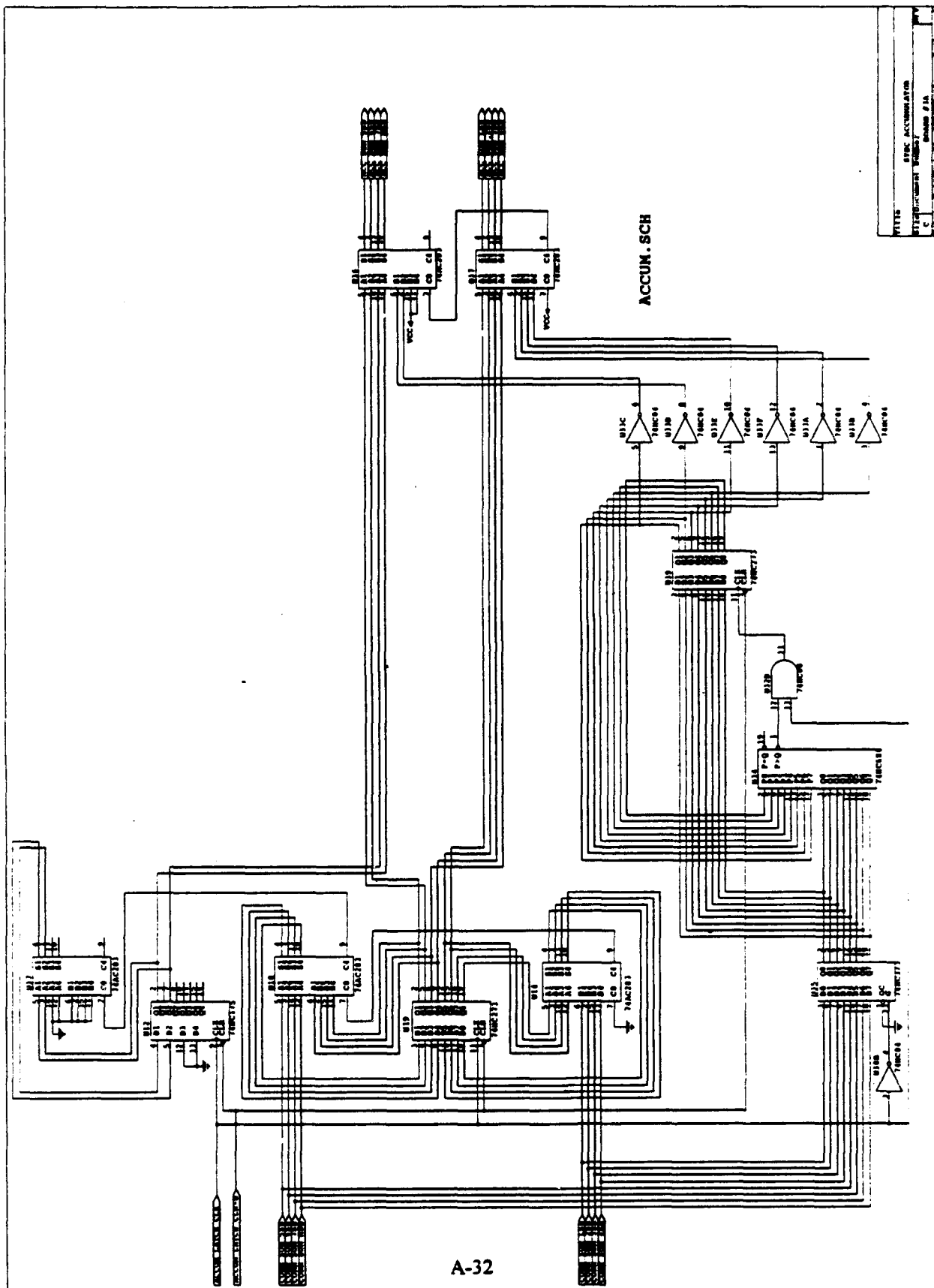
END OF DATA FILE

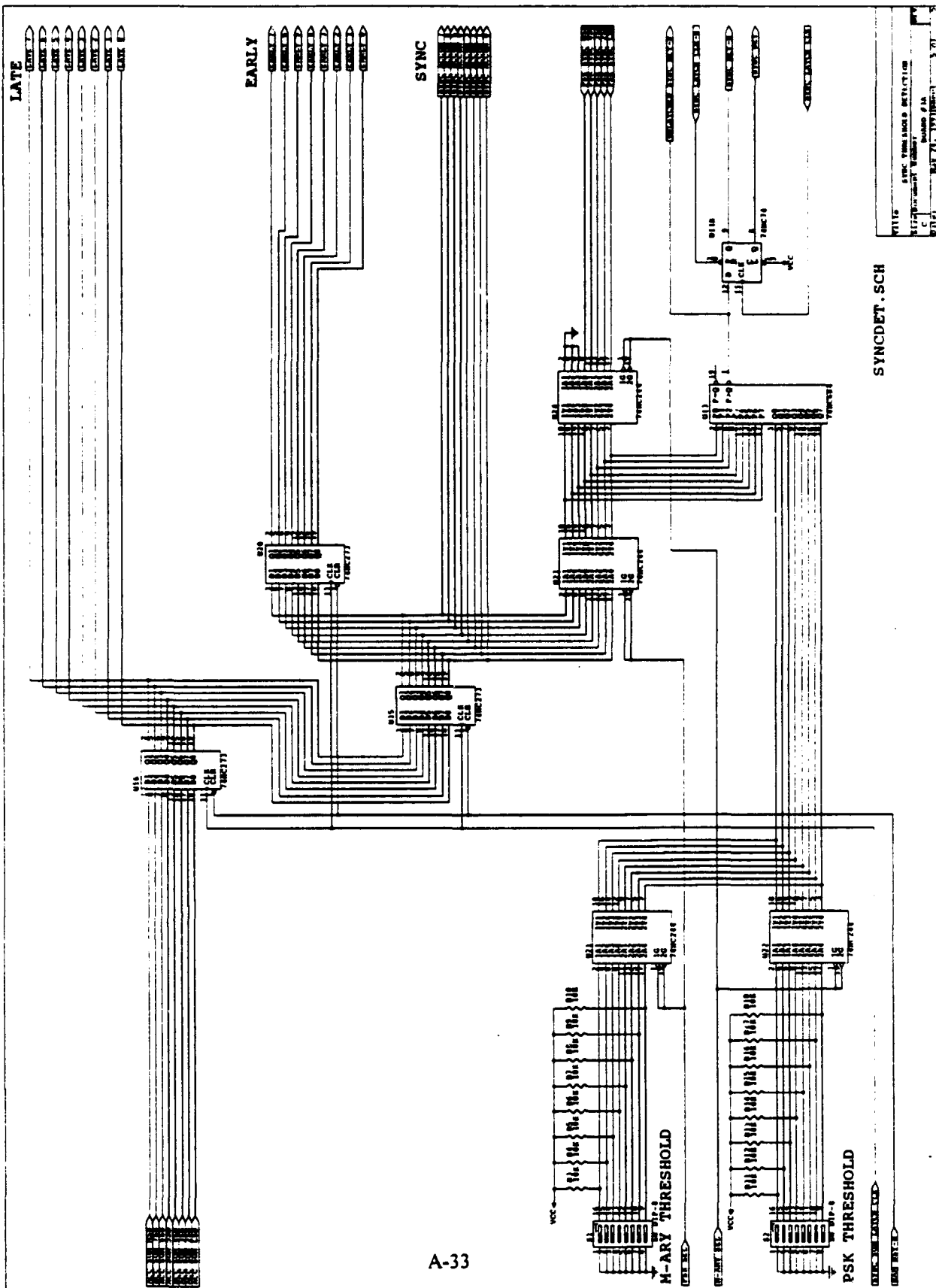


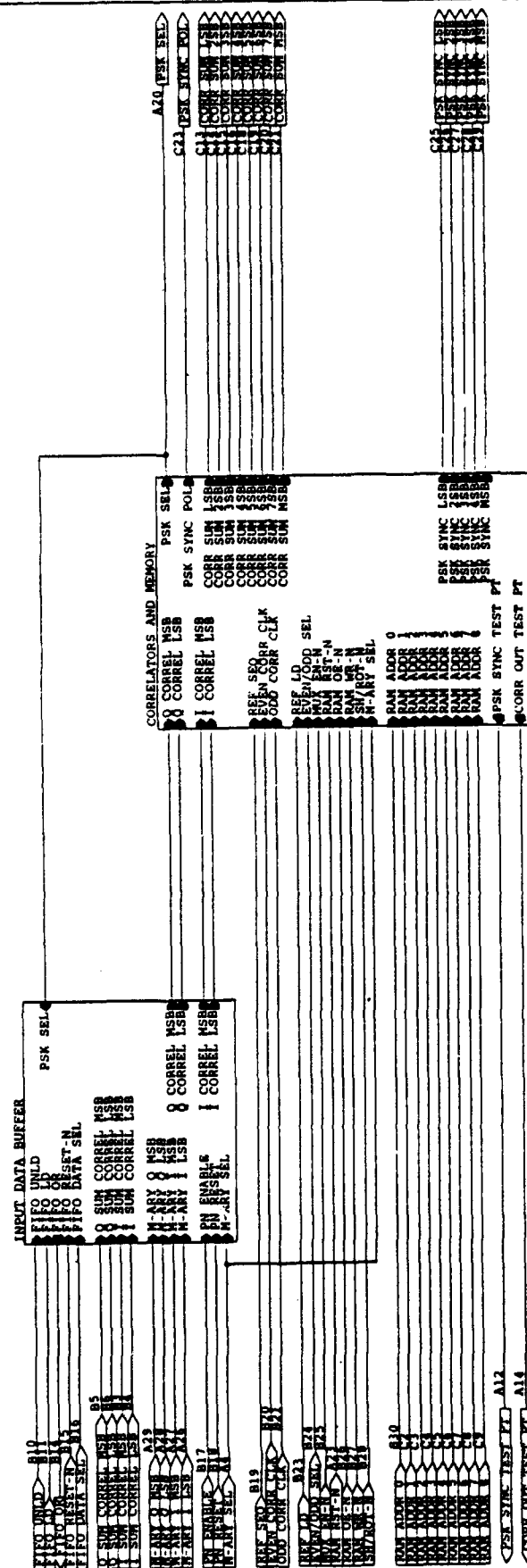
TITLE: 74181 ALU
 STATUS: Final
 DATE: February 11, 1978
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DB25M



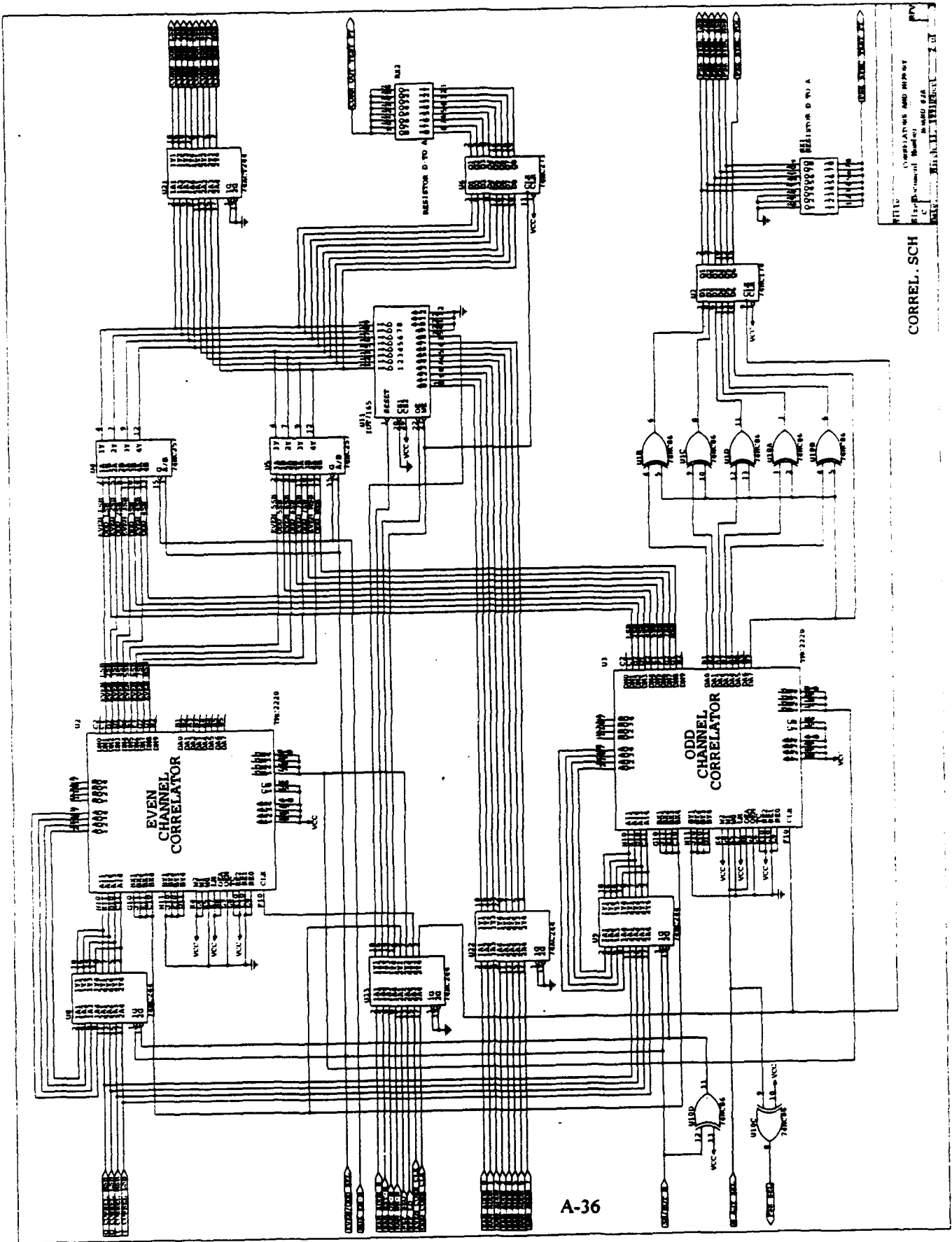






SLOT A06
CORRBUFF.SCH

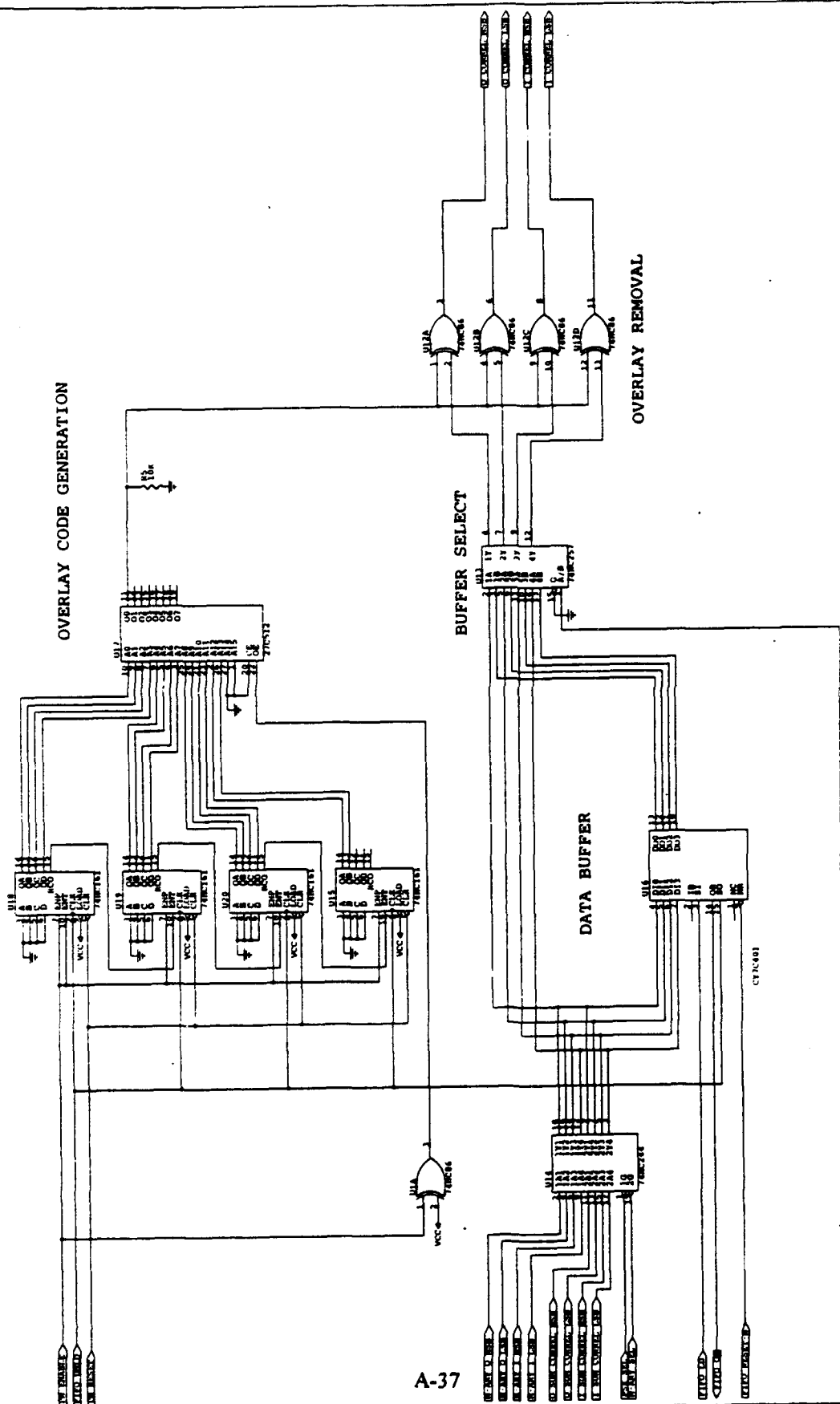
Title _____
Size Document Number _____
Date _____
RAIC _____
REV _____



A-36

DATE: 06/11/65
DESIGNED BY: J. A. HARRIS
CHECKED BY: J. A. HARRIS
APPROVED BY: J. A. HARRIS

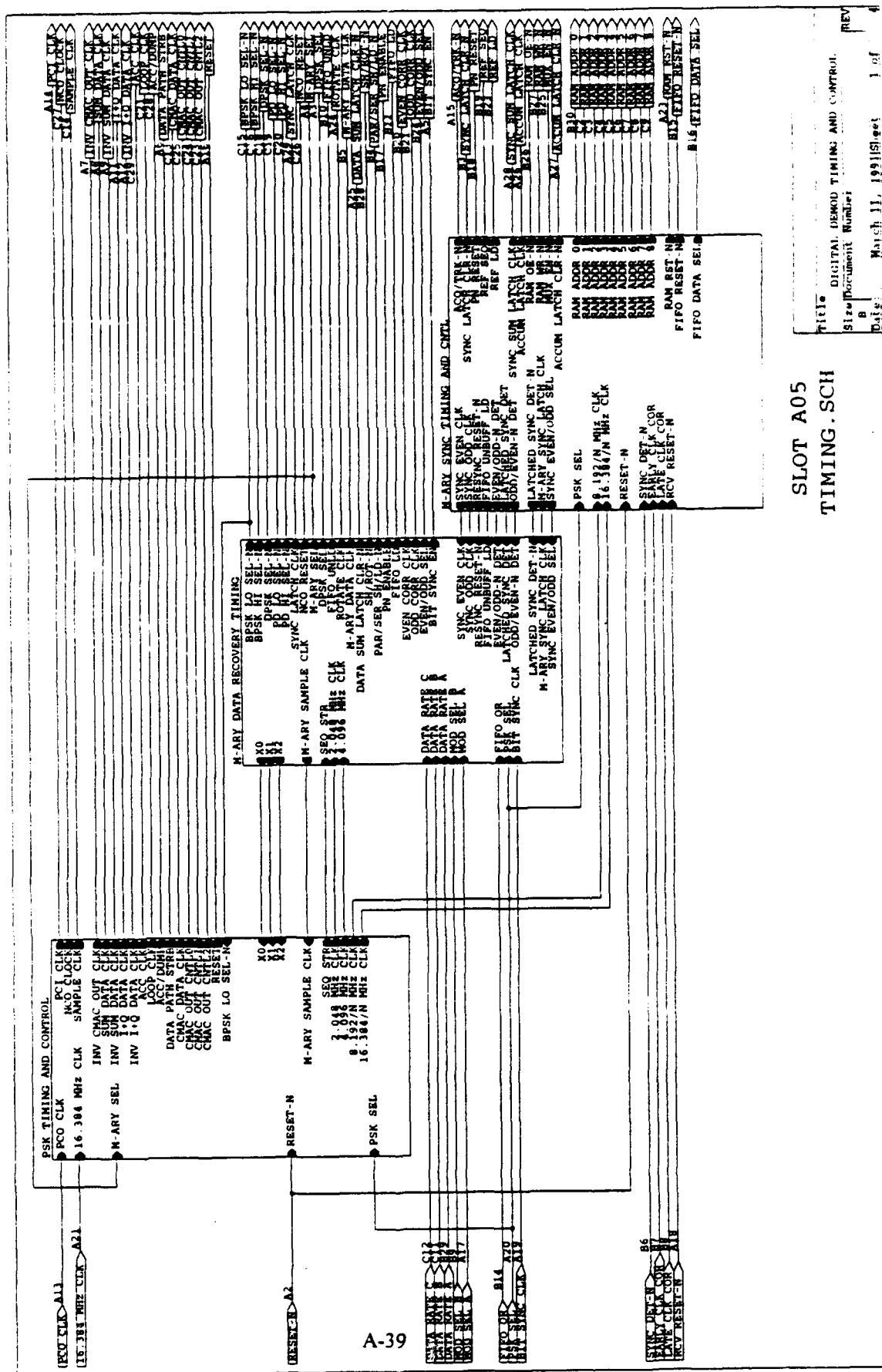
CORREL. SCH



MARYFIFO.SCH

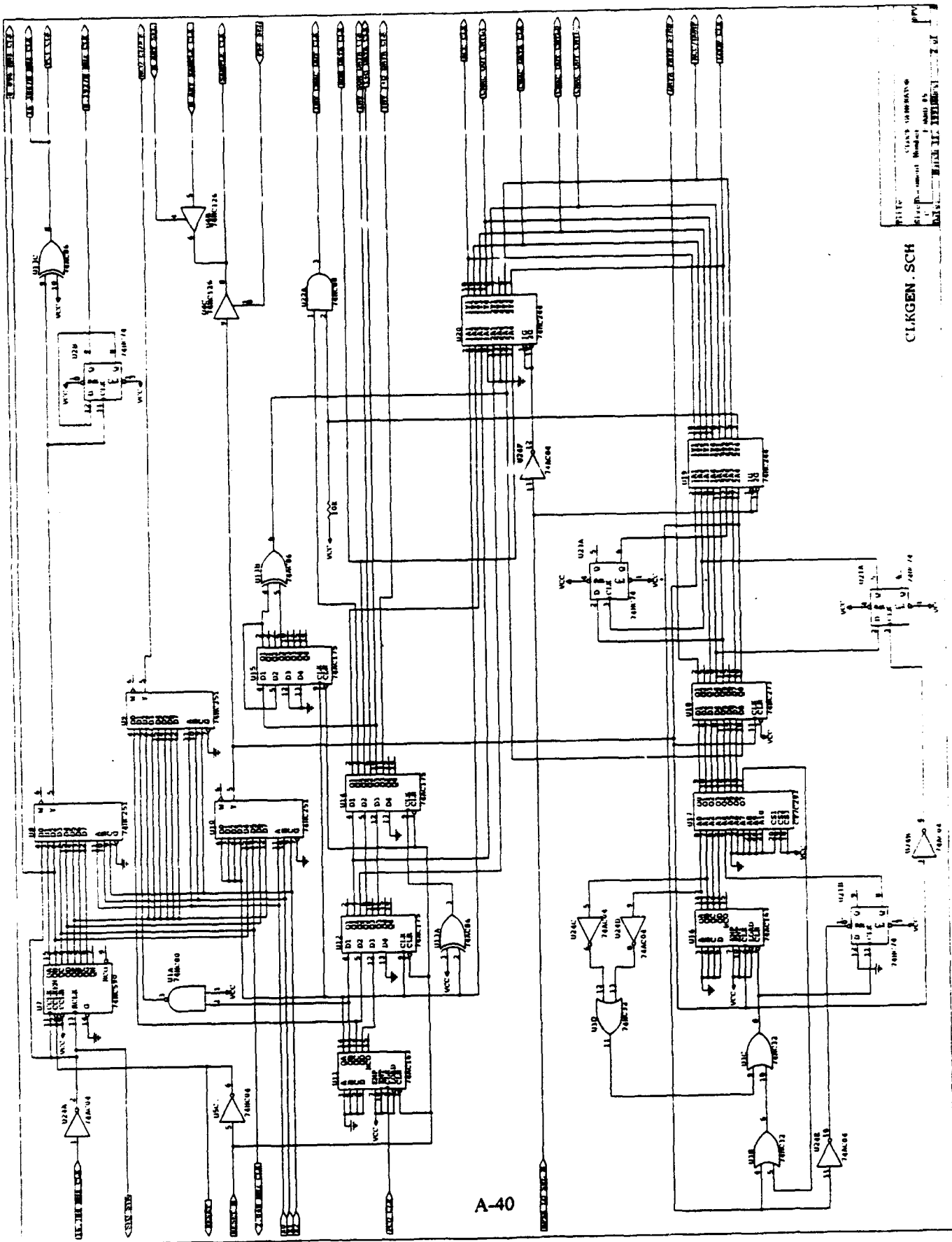
DATE: 10/10/81
 DESIGNED BY: J. J. JENSEN
 CHECKED BY: J. J. JENSEN
 APPROVED BY: J. J. JENSEN
 TITLE: MARYFIFO.SCH

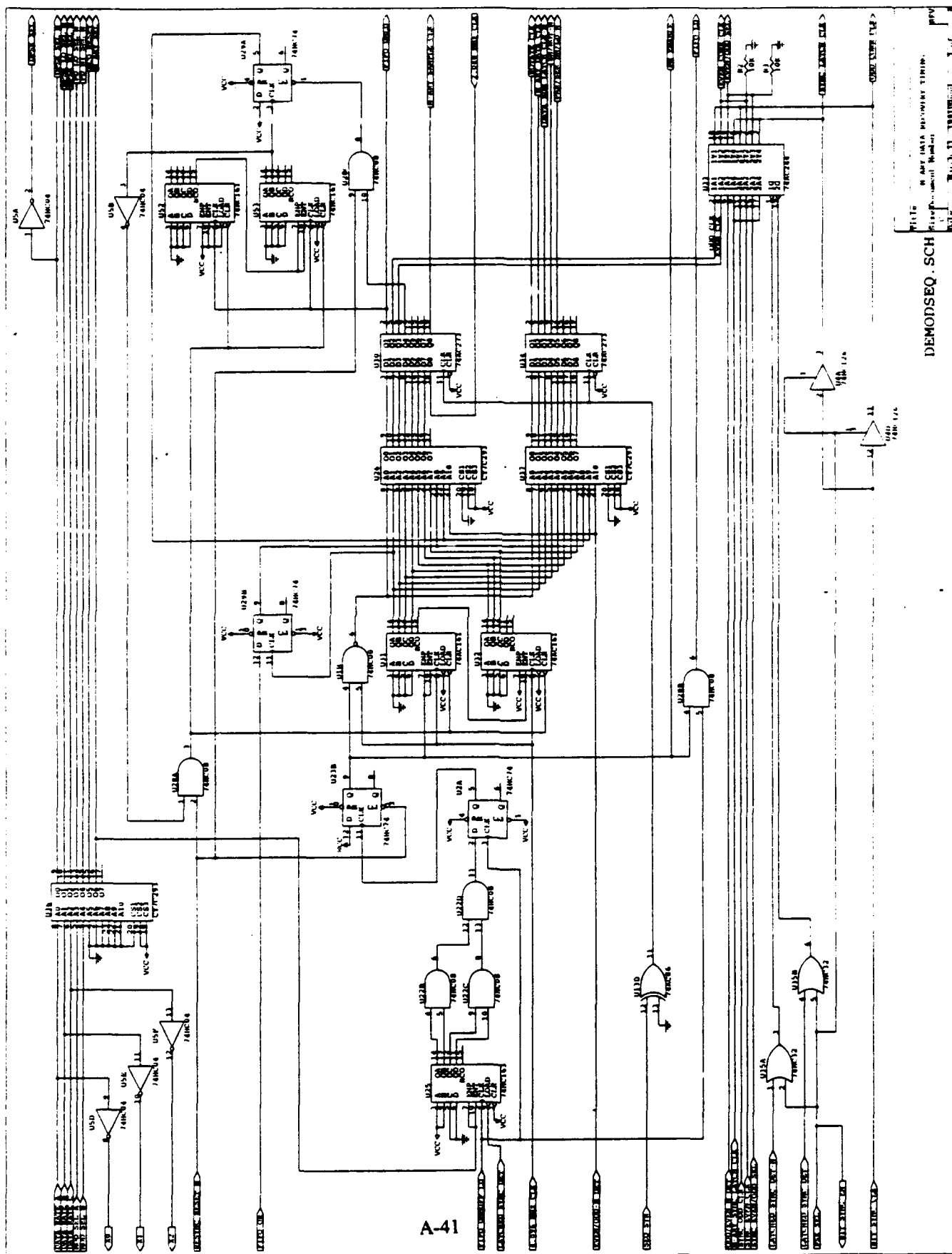




DATE: 01/11/84
 DESIGNED BY: J. J. J. J. J.
 CHECKED BY: J. J. J. J. J.
 DRAWN BY: J. J. J. J. J.

CLKGEN.SCH





INITIALIZATION & SYNC SEQUENCER

A-42

RAM ADDRESS EPROM

CORR CLK EPROM

RAM & LATCH CNTL EPROM

COUNTER LATCH

U400 74AC04

U401 74AC04

U402 74AC04

U403 74AC04

U404 74AC04

U405 74AC04

U406 74AC04

U407 74AC04

U408 74AC04

U409 74AC04

U410 74AC04

U411 74AC04

U412 74AC04

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U604 74AC04

U605 74AC04

U606 74AC04

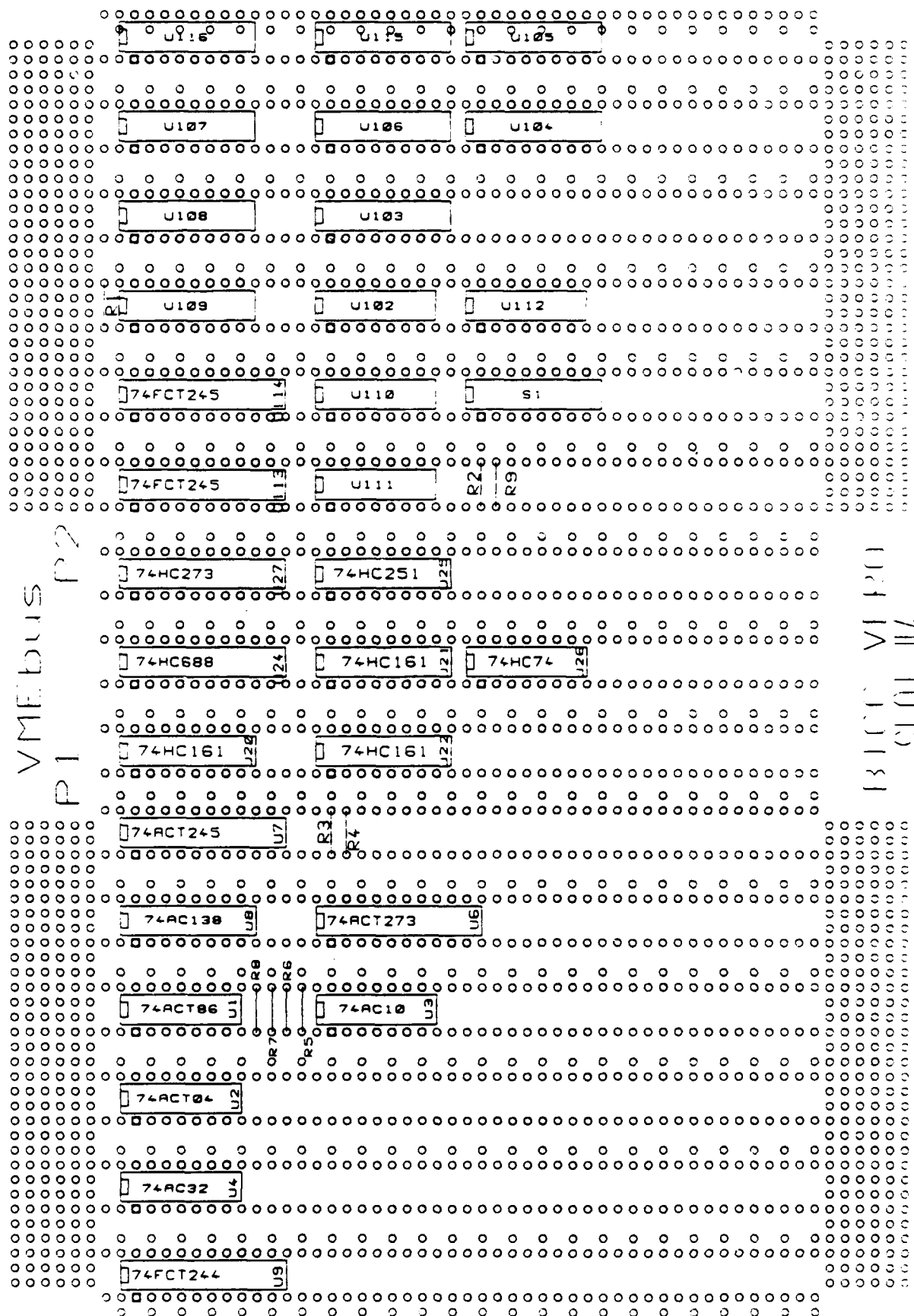
U607 74AC04

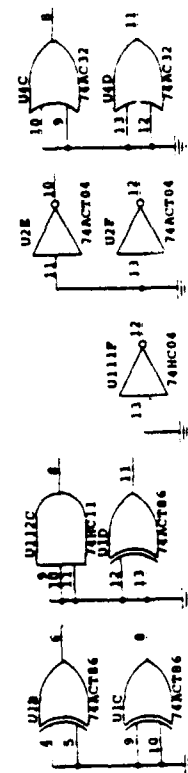
U608 74AC04

U609 74AC04

U610 74AC04

[illegible][illegible][illegible]

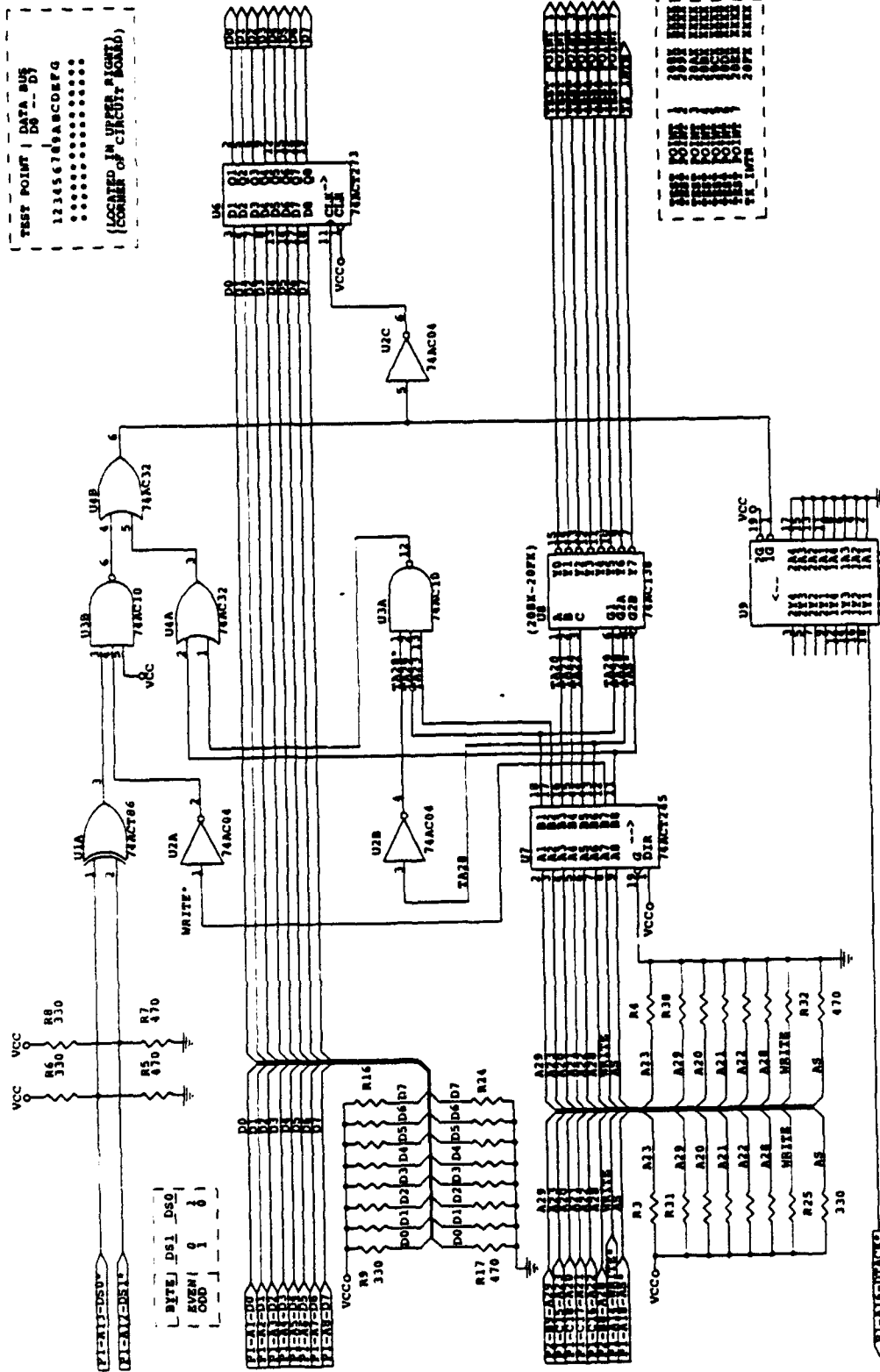




117-ACD
RODNEY L. WILSON
1919 W. COOK RD.
FORT WYOMING, IN. 46901

HCS 0170-SCH

TEST POINT | DATA BUS
D0 -- D7
123456789ABCDEF
.....
.....
(LOCATED IN UPPER RIGHT)
(CORNER OF CIRCUIT BOARD)



VCC
GND

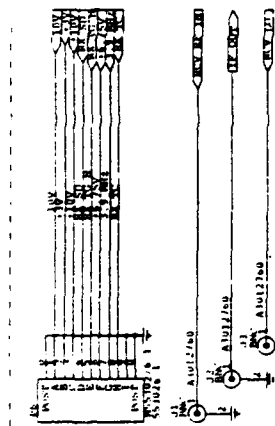
17T-MCD
ROONEY L. WILSON
1919 W. COOK RD.
PORT WATNE, IN. 46081

TITLE
CIRCUITRY
TEST POINT
F30602-89-C-0024-2
REV
DATE: FEBRUARY 1, 1977

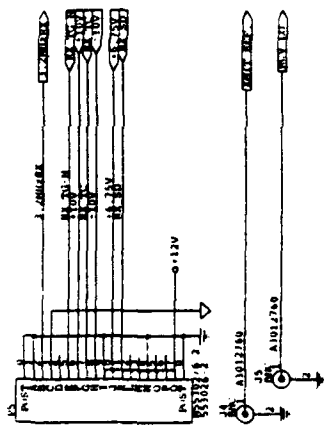
TEST_PT.SCH



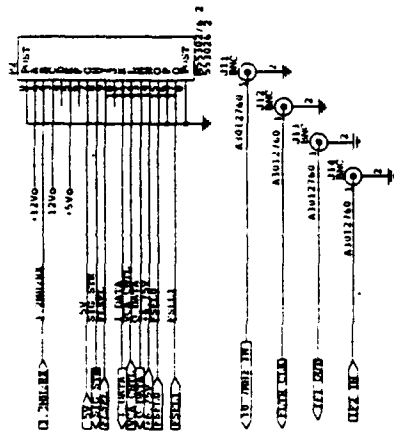
ITT-ACD	ROONEY L. WILSON	PROGRAMMABLE TR FIPO
	1919 W. COOK RD.	
	FORT WAYNE, IN. 46801	
TITLE		
SECRET DOCUMENT NUMBER		
D	F36002-89-C-0024-2	
DATE	FEBRUARY 1, 1975	



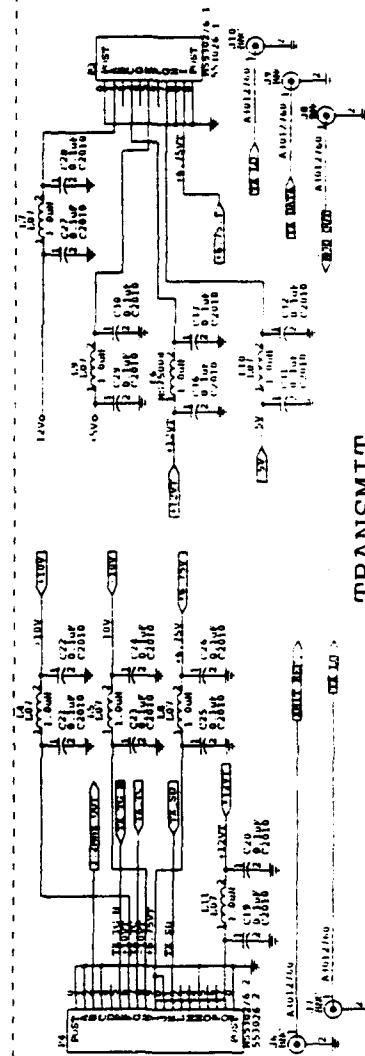
TUNER/MIXER



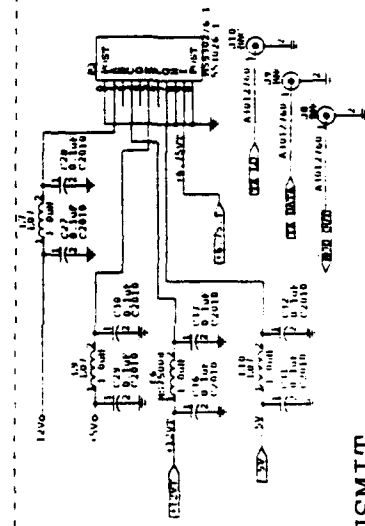
RECEIVE SYNTHESIZER



IF/DEMOD

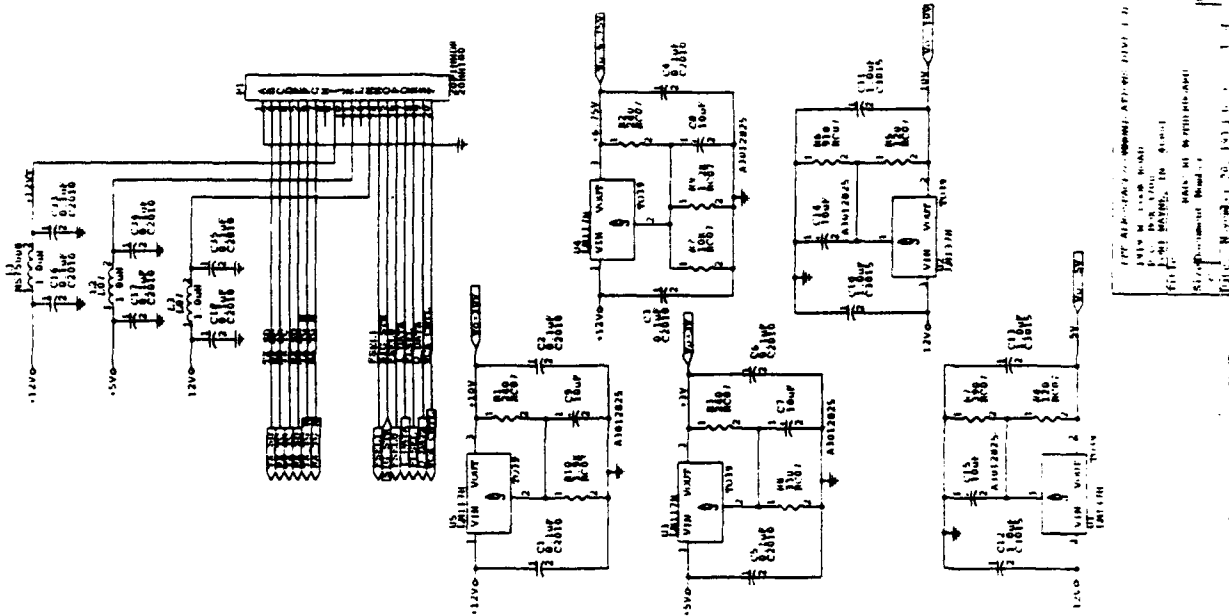


TRANSMIT SYNTHESIZER

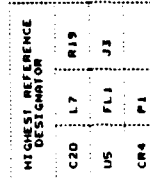


MODULATOR

TRANSMIT SECTION

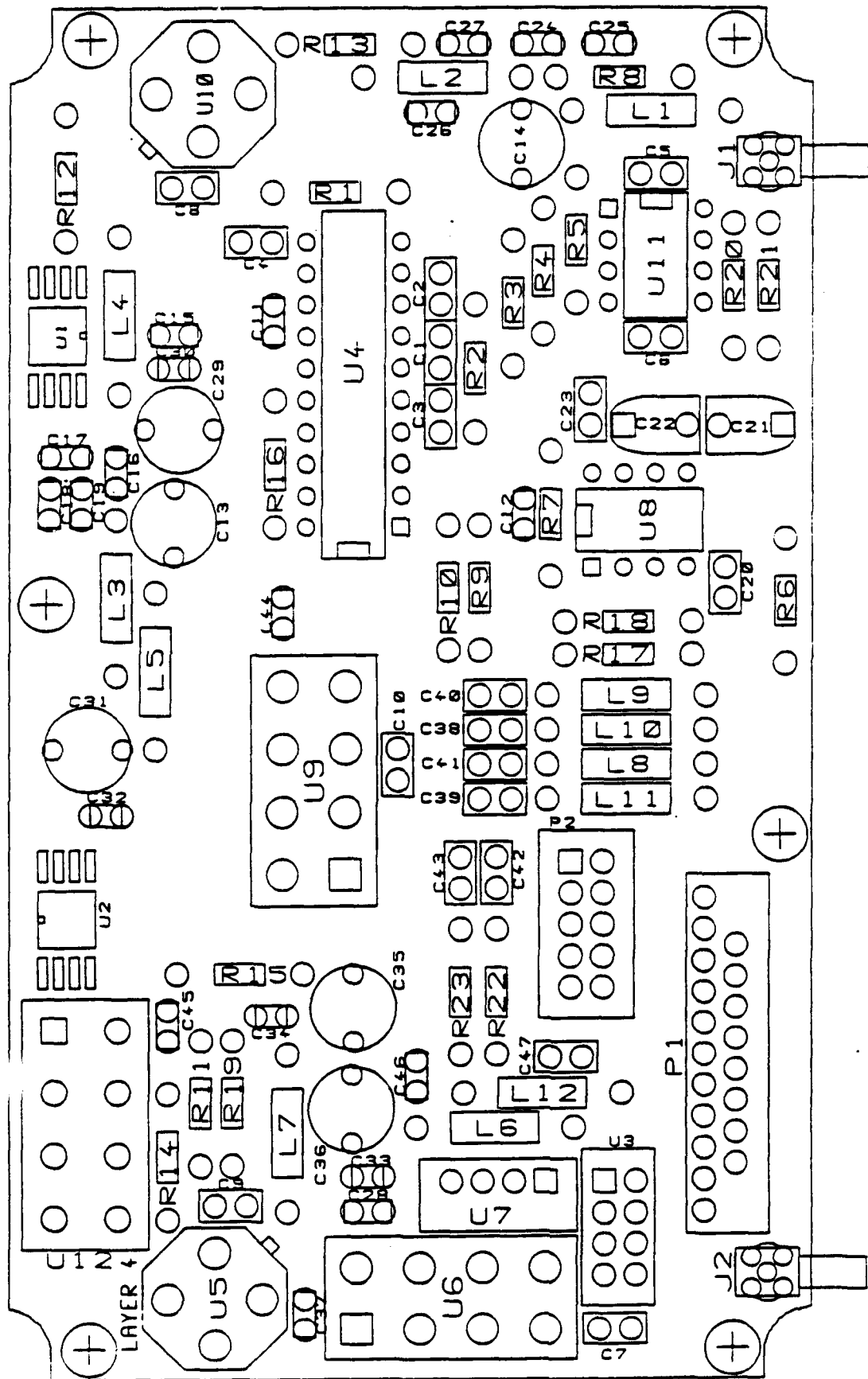


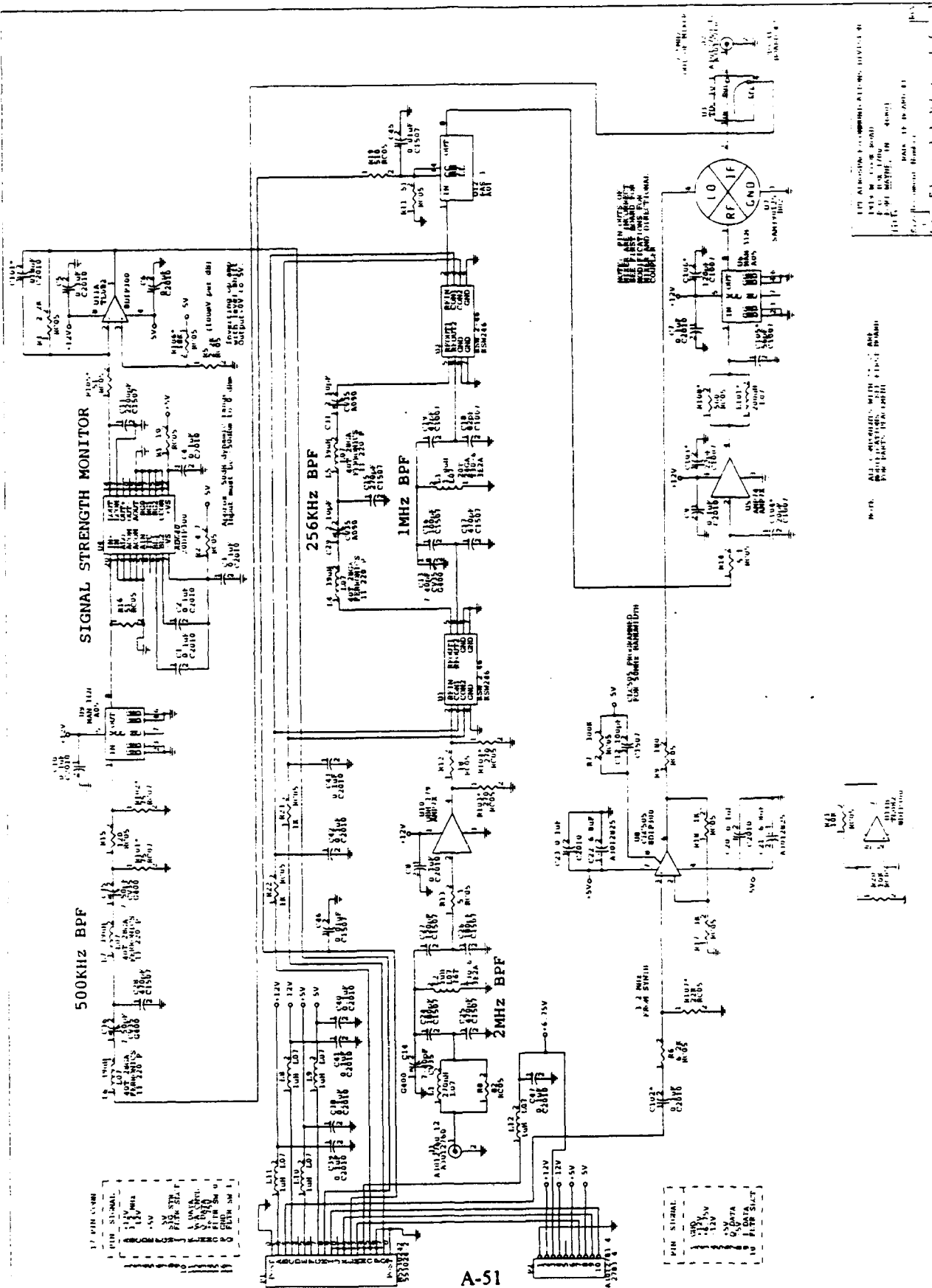
100% ALUMINUM COMMUNICATIONS, INC. 100%
100% ALUMINUM COMMUNICATIONS, INC. 100%
100% ALUMINUM COMMUNICATIONS, INC. 100%
100% ALUMINUM COMMUNICATIONS, INC. 100%
100% ALUMINUM COMMUNICATIONS, INC. 100%



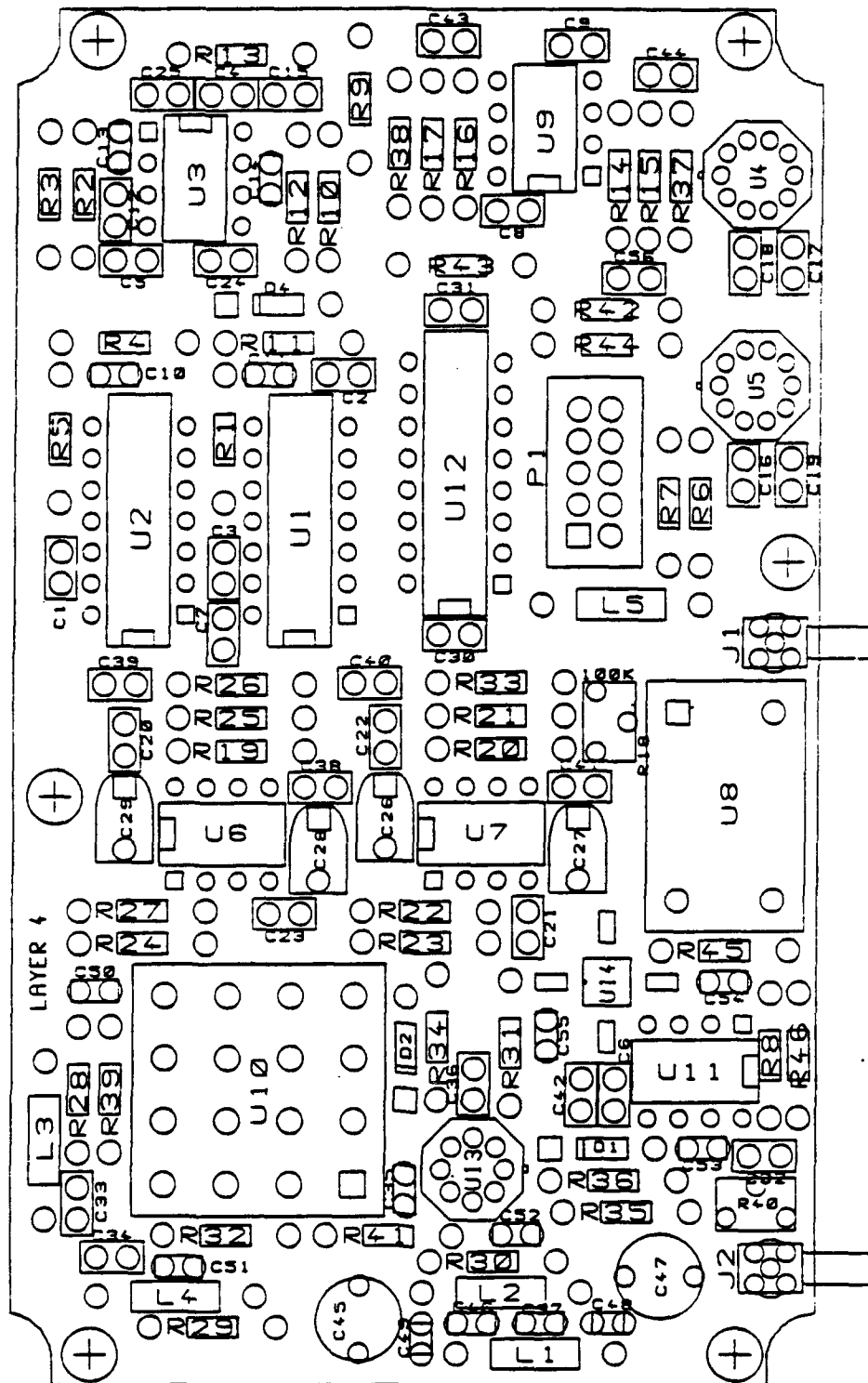
1950

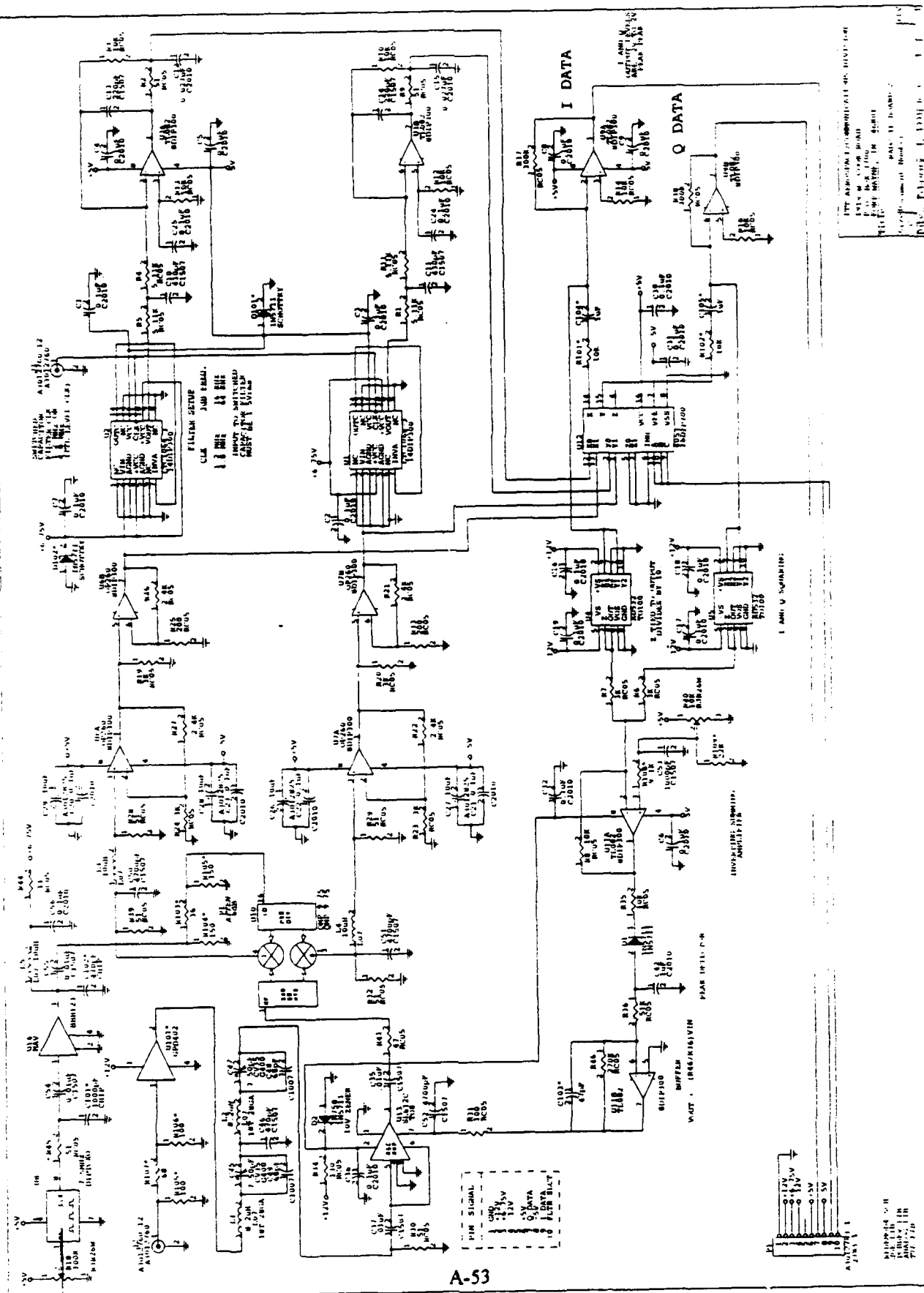
Layout for IF Board 1



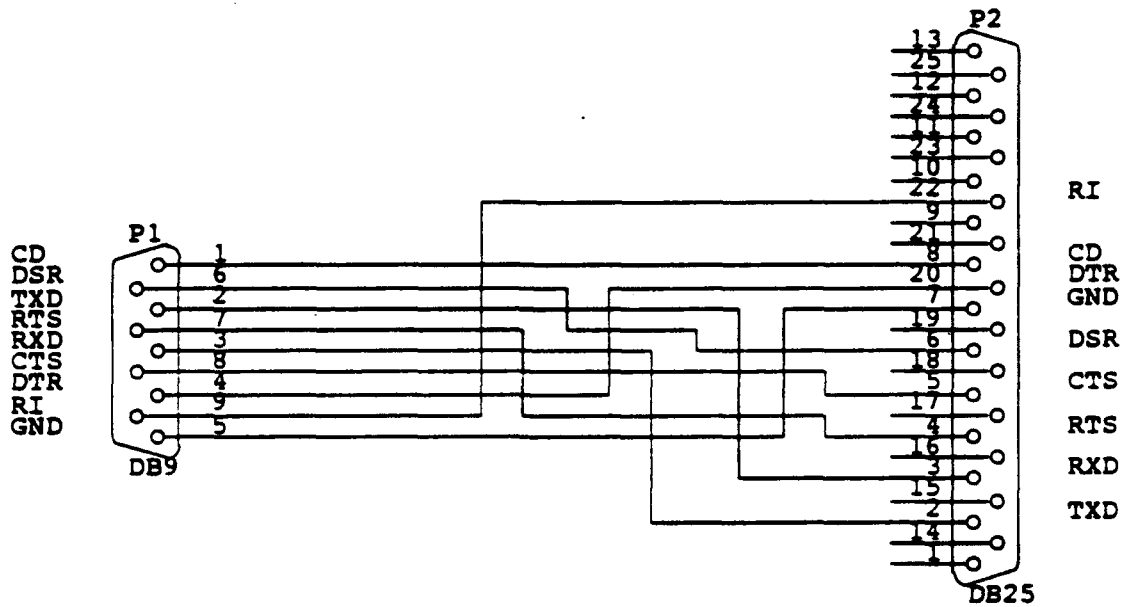


Layout for IF Board 2

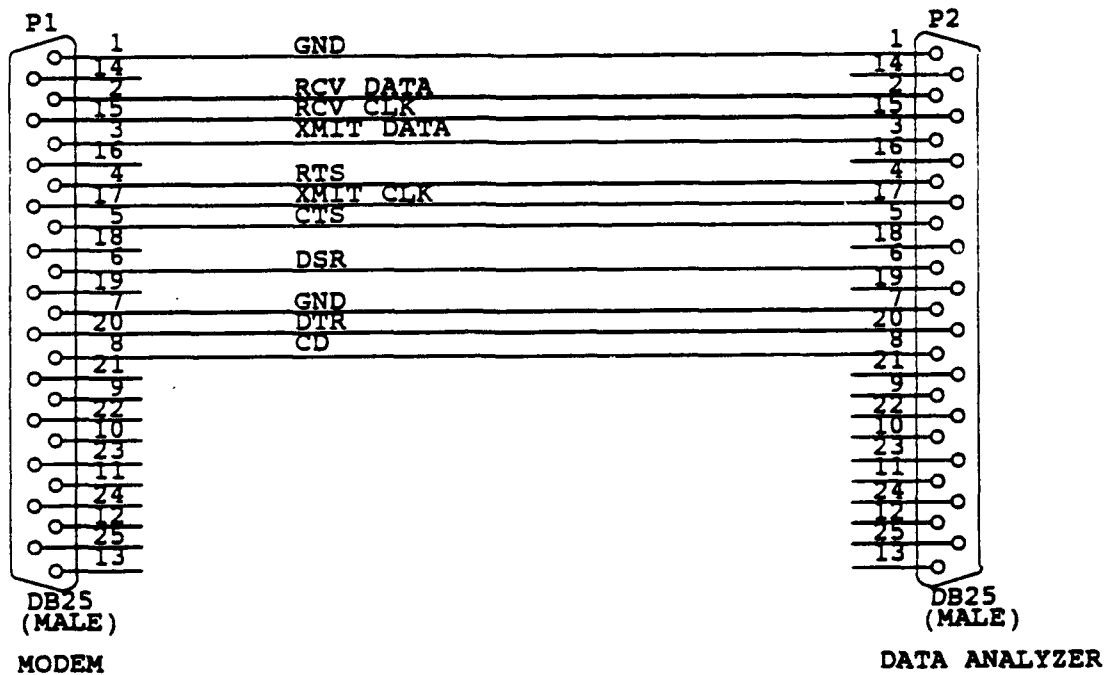




RS-232 Cable - Modem to Control Terminal



BER Loop Back Test Cable



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